Trade-Off Relationship of Size and Density of Platinum Nanocrystal in Nonvolatile Memory Characteristics

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The replacement of metal nanocrystal (NC)-based nonvolatile memories (NVMs) with polycrystalline silicon floating-gate memories is very attractive, since they demonstrate superior capability of charge localization and a reduction in cell-to-cell interference. Varying the size (ranging from 15.1 to 55.2 nm) and density (from 5.6×10^{11} to 3.2×10^{10} cm^{-2}) of the metal NC affects the entire memory properties such as the charging/discharging process, retention characteristic, and charge storage capability. Here, we investigated the effects of the size and density of platinum (Pt) NCs on the aforementioned memory characteristics by fabricating Pt-NC-embedded metal oxide semiconductor (MOS) capacitors using a direct self-assemble method. The flatband voltage shift, a measure of charge storage capability for NC-based NVMs, increased from 5.75 to 13.05 V as the mean size of the NCs was varied from 15.1 to 55.2 nm, which was relatively higher than that of other NC-based NVMs. Our studies revealed that the flatband voltage shift depends on not only the size and density of the NCs, but also the tunneling probability of the electrons, which is closely related to the applied electric field at a tunneling oxide. The relationships among the flatband voltage shift, the size and density of the NCs, and the applied electric field, which are revealed in this study, can be generally applicable to other NVMs based on various metal and semiconducting NCs.

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1. Introduction

Nonvolatile memories (NVMs) using a discrete charge storage node for the floating gate have received much attention as a promising candidate for the replacement of the conventional polycrystalline silicon (poly-Si) floating-gate memory, owing to their higher operation speed, longer retention time, lower power consumption, better endurance, and especially, their charge localization capability, which enable the aggressive scaling of tunneling oxide and the reduction of the cross-talk between cells.[1–3] Various materials have been investigated for discrete floating gates in recent years, which include amorphous silicon (a-Si),[4] silicon nitride (SiN),[5,6] oxygen-incorporated silicon carbide (SiC),[7,8] semiconductor and metal nanocrystals (NCs),[9–13] and C_{60} nanocomposites.[14] Among the aforementioned materials, memories using a metal NC floating gate are considered to be more advantageous in many aspects over silicon (Si)-NC-based memories, since metal-NC floating-gate memories made of metals with relatively high work functions such as platinum (5.65 eV) and gold (5.1 eV) can achieve higher density of states, a stronger coupling with the conduction channel, a higher program/erase speed, and a longer retention time.[11]

The performance of NC-based NVMs is highly affected by two dominant factors: the size and the density of the NCs. Generally, the use of high-density and large NCs with minimal fluctuation in their shapes leads to better memory characteristics with a large memory window. However, owing to the trade-off relationship between the size and density of NCs, it is impossible to realize of a high density of NCs with a large size in a limited area. Many studies have been conducted to controllably manipulate the size and density of NCs separately so as to find the optimal relationship between the two parameters leading to a higher performance of NVMs. The relationship, however, still remains unclear owing to the fact that it is very difficult to independently control one factor without affecting the other.[15–20] Thus, an investigation on the combined effects of the dominant factors is expected to lead to a new method of fabricating NVMs with great potential.

In this paper, we report the effects of the size and density of platinum (Pt) NCs embedded inside a silicon dioxide (SiO_2) layer on the electrical characteristics of a NVM capacitor. Using a direct self-assemble process, four different sets of specimens were prepared by varying the size and density of Pt NCs, from 15.1 to 55.2 nm, and 5.6×10^{11} to 3.2×10^{10} cm^{-2}, respectively. The memory properties including the charging/discharging process, retention property, and charge storing capacity of a metal oxide semiconductor (MOS) capacitor with various the sizes and densities of Pt NCs were studied. The results showed that the flatband voltage shift and retention property depend on the size (their density is inversely proportional to the size) of the NCs, and that the charge storage capacitance per NC is linearly dependent on the surface area of the NCs.

2. Experimental Methods

MOS capacitors with a Pt NC floating gate were fabricated on (100)-oriented p-type Si substrates (1–10 Ω·cm). A 4.5-nm-thick tunneling SiO_2 layer was thermally grown at 800 °C in a dry oxidation furnace. To fabricate Pt NCs on the tunneling oxide layer, a thin Pt wetting layer was deposited on the oxide layer by dc magnetron sputter deposition at a deposition rate of 1.17 Å·s^{-1} and a working pressure of 5×10^{-3} Torr. A rapid thermal annealing (RTA) process was then carried out in nitrogen (N_2) ambient to deform the thin Pt wetting layer into NCs, under 800 °C for 30 s. In order to examine the effects of the size and distribution of the NCs on the memory characteristics, a series of samples with four different initial Pt film thicknesses of 2, 4, 6, and 8 nm were prepared by the aforementioned film deposition process, followed by the RTA process. A 60-nm-thick SiO_2-based control oxide layer was then deposited by plasma-enhanced chemical vapor deposition (PE-CVD) at a substrate temperature of 300 °C and growth rate of 18.3 Å·s^{-1}. Finally, aluminum (Al) gate electrodes with a circular pattern and a diameter of 600 μm were deposited on top of the control oxide to a thickness of 200 nm.

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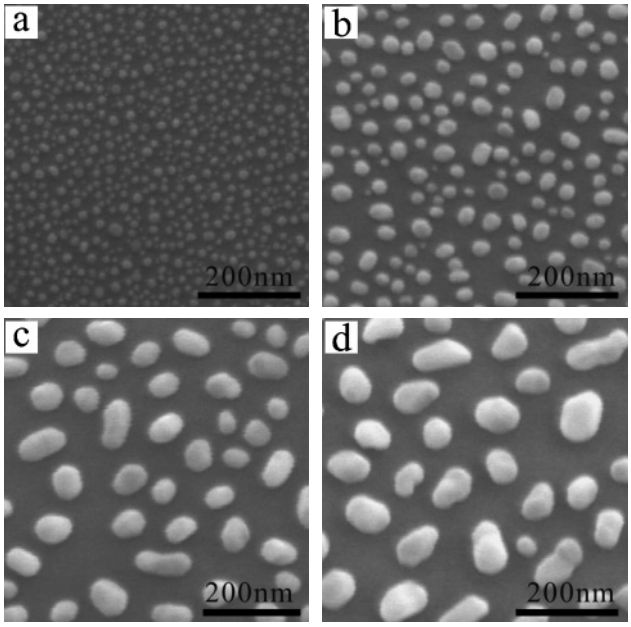

Fig. 1. Typical SEM images (600 × 600 nm^2) of Pt NCs fabricated on top of tunneling oxide by RTA process, whose the initial as-deposited Pt film thicknesses are, (a) 2, (b) 4, (c) 6, and (d) 8 nm.

The morphology of the Pt NCs was investigated using a Hitachi S-4300 field emission scanning electron microscope (FE-SEM) and a tapping-mode Veeco NanoScope IV atomic force microscope (AFM), in which several $1 \times 1\,\mu m^2$ area scans were obtained from each sample. The memory characteristics of the MOS capacitor were investigated by capacitance–voltage (C–V) measurement at a 1 MHz frequency using a Keithley 590 C–V analyzer. The charge retention properties of the capacitor with various sizes and densities of Pt NCs were investigated by the transient–capacitance (C–t) measurement method.

3. Results and Discussion

Figure 1 shows typical SEM images ($600 \times 600\,nm^2$) of the NCs on top of the tunneling oxide layer for four different MOS capacitor configurations with initial Pt film thicknesses of (a) 2, (b) 4, (c) 6, and (d) 8 nm. The as-deposited Pt films on the thermally grown tunneling oxide were converted into the NCs through the RTA process at 800 °C for 30 s in N_2 ambient. The formation of Pt NCs was a direct result of an energy minimization process, where the stress induced in the Pt thin films during their deposition was relieved as a result of the thermal energy provided in the RTA process. Consequently, the Pt films were transformed into isolated NCs to lower the surface energy. The perturbation in the thickness of the as-deposited Pt layer caused the initial formation of nuclei of the NCs during the RTA process. Further isolation and the subsequent following coalescence process of the NCs were limited by the surface mobility of the metal atoms.[15,21] The exact morphologies of the NCs, which were obtained by AFM analysis (not shown in this paper), were shown to be hemispherical dots. For the samples with initial Pt film thicknesses of 2 and 4 nm, the NCs were well distributed and separated from one another by an approximately equal (≅20.3 and 34.7 nm for 2 and 4 nm Pt film thicknesses, respectively), and their mean sizes

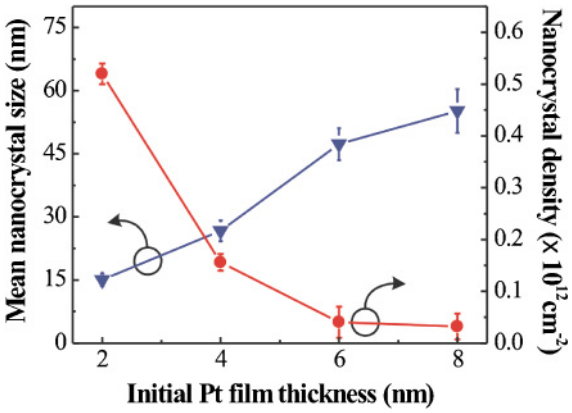

Fig. 2. (Color online) Variations in mean NC size and density as a function of the initial deposited Pt film thickness. The sizes of NCs ranged from 15.1 to 55.2 nm (shown on left Y-axis) and the densities of NCs ranged from 3.2×10^{10} to $5.6 \times 10^{11}\,cm^{-2}$ (shown on right Y-axis).

were about 15.1 ± 2.91 and 26.7 ± 4.94 nm, respectively. On the other hand, as the thickness of the as-deposited Pt films increased to 6 and 8 nm, the size of the NCs had relatively large variations owing to the poor isolation of the NCs. It was observed that some of the NCs merged together by ripening and coalescence processes, leading to the formation of an elliptical shape rather than a good hemispherical shape. However, the fraction of the elliptical NCs is large. Thus, the presence of the elliptical NCs may weakly affect the memory characteristics, and it is assumed that the Pt NCs are uniformly distributed and hemispherical for simplicity in further analysis.

Figure 2 shows a plot of the changes in the size and density of the Pt NCs as a function of the as-deposited Pt film thickness ranging from 2 to 8 nm. The size of the NCs increased proportionally with increasing thickness of the as-deposited Pt film, while the density of the NCs was inversely proportional to the Pt film thickness. The mean size of the Pt NCs increased from 15.1 to 55.2 nm and their density decreased from 5.2×10^{11} to $3.2 \times 10^{10}\,cm^{-2}$ as the as-deposited Pt film thickness varied from 2 to 8 nm. From preliminary experiments, it has been revealed that the NCs generated from Pt films thicker than 10 nm were not fully isolated and had distorted shapes; such results were excluded for the analysis of the effects of the size and density of the NCs. These results indicate that the size and density of the NCs depend on the thickness of the as-deposited film, similarly to the results of previous studies investigation on the effect of film thicknesses.[21,22]

Figures 3(a)–3(d) show the charging characteristics of Pt-NC-based memories with different NC sizes. For the measurements, a DC bias was swept from a negative bias (−20 V) to a positive bias (+20 V) and then swept back to the original negative bias. When a positive bias was applied to the gate electrode, electrons were injected into the Pt NCs from the inversion layer of the Si substrate by a tunneling mechanism. In contrast, a negative bias caused the ejection of the stored electrons from the Pt NCs. Consequently, the electrons injected in the Pt NCs shifted the C–V curve in the positive direction, resulting in a counterclockwise hysteresis loop. At an applied sweep voltage of 40 V (±20 V), ΔV_{FB} increased from 5.75 to 13.05 V as the mean size of NCs

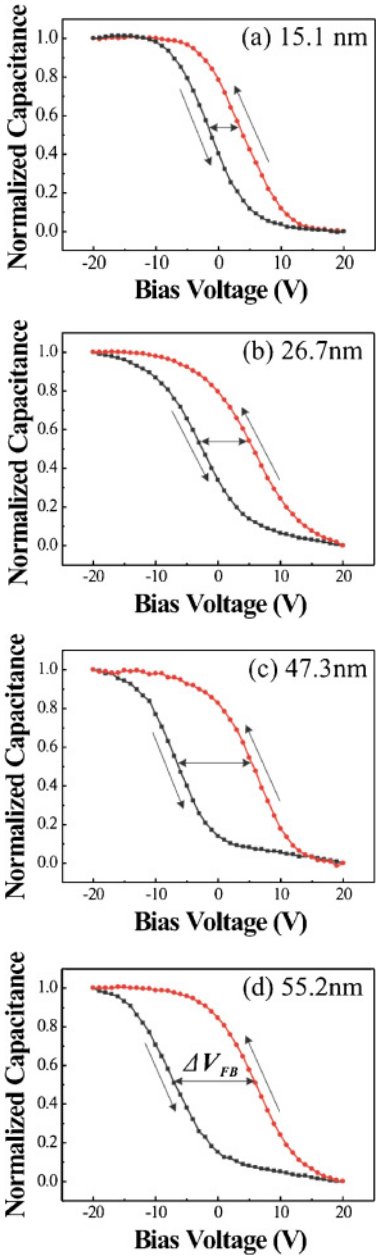

Fig. 3. (Color online) High-frequency (1 MHz) *C–V* curves under ±20 V forward and backward sweep conditions for NVM capacitors with NCs having mean sizes of (a) 15.1, (b) 26.7, (c) 47.3, and (d) 55.2 nm.

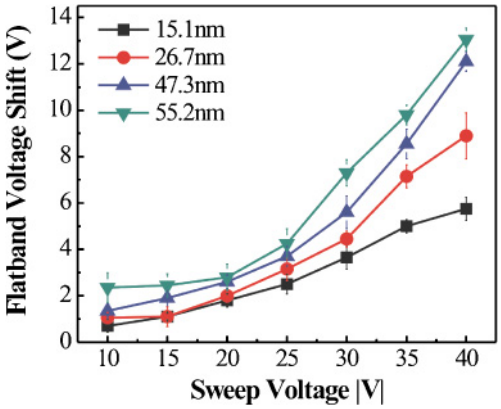

Fig. 4. (Color online) Flatband voltage shift as a function of sweep bias voltage from 10 V (±5 V) to 40 V (±20 V) for NVM capacitors with varying NC size.

Table I. Comparison of E_{ox} and corresponding values of ΔV_{FB} of NC-based memories.

NC	Mean NC size (nm)	Density (cm^{-2})	E_{ox} (MV/cm)	ΔV_{FB} (V)
Si[24]	8	4×10^{11}	3.57	1.8
Au[25]	6.26	4.08×10^{11}	1.88	6.5
Pt[26]	3	3×10^{12}	6.67	3.2
Pt	15.1	5.6×10^{11}	3.31	5.75

increased from 15.1 to 55.2 nm. Considering the fact that a negligible hysteresis loop was obtained for the MOS capacitor without the NCs ($\Delta V_{FB} \cong 0.4$ V), we suggest that Pt NCs have a higher capability of storing electrical charges, evidenced by the hysteretic curve of the *C–V* measurement in Fig. 3. The ΔV_{FB} gradually increased with the size of the NCs, which was primarily due to the fact that larger NCs are capable of holding more electrical charges than smaller NCs. Since the ΔV_{FB} is closely related to the number of electrons stored inside the memory capacitor, a large hysteresis loop can be beneficial to identifying the 0 and 1 states.

Figure 4 shows the variation in ΔV_{FB} with increasing sweep bias voltage from 10 V (±5 V) to 40 V (±20 V) for MOS capacitors with different sizes of NCs embedded on the SiO_2 layer. The sweep bias voltages lower than 10 V were not included in the data analysis since the ΔV_{FB} was negligible and similar to that obtained from the MOS capacitor without the NCs. As shown in Fig. 4, an exponential relationship was observed between the ΔV_{FB} and the applied sweep voltage, which can be characterized by the charge transport current of the Fowler–Nordheim (FN) tunneling mechanism as follows:[23]

$$J_{FN} = \frac{q^3}{8\pi h \phi_b} E_{ox}{}^2 \exp\left[-\frac{8\pi(2m_{ox})^{1/2}\phi_b{}^{3/2}}{3qhE_{ox}}\right], \quad \text{for } V_{ox} > \phi_b, \qquad (1)$$

where q is the magnitude of a single electronic charge, h is the Planck constant, ϕ_b is the tunneling barrier of the tunneling oxide, E_{ox} is electric field across the tunneling oxide, m_{ox} is the effective mass of oxide, and V_{ox} is the voltage drop at the tunneling oxide. Here, the electric field across the tunneling oxide can be estimated by $E_{ox} = V_{ox}/t_{ox}$, where t_{ox} is the thickness of the tunneling oxide. As described in eq. (1), the tunneling current density is proportional to the square of the applied electric field; therefore, ΔV_{FB} exponentially increased with the sweep bias voltage. However, since the rate of increase was lower as the size of the embedded NCs decreased, the difference in the ΔV_{FB} for the four different sets of specimens became larger with increasing sweep voltage. The slow rate of increase for the smaller NCs can be ascribed to the low capability of charge storage in the smaller NCs.

For a comparative analysis, ΔV_{FB} and E_{ox} were extracted from previous reports on Si-, Au-, and Pt-NC-based memories[24–26] and are summarized in Table I. The Si-NC-based memory showed a rather poor ΔV_{FB} of 1.8 V at $E_{ox} = 3.57$ MV/cm for a mean size of 8 nm and a density of 4×10^{11} cm^{-2}. On the other hand, an improved ΔV_{FB} of 6.5 V was obtained for Au-NC-based memory at

$E_{ox} = 1.88\,\mathrm{MV/cm}$ for a mean size of 6.26 nm and a density of $4.08 \times 10^{11}\,\mathrm{cm}^{-2}$; in the case of the Pt-NC-based memory, the measured ΔV_{FB} was 3.2 V at $E_{ox} = 6.67\,\mathrm{MV/cm}$ for a mean size of 3 nm and a density of $3 \times 10^{12}\,\mathrm{cm}^{-2}$. Thus, it is clear from the comparison that our Pt-NC-based memory shows a similar or larger ΔV_{FB}, i.e., 5.75 V, at $E_{ox} = 3.31\,\mathrm{MV/cm}$ for a mean NC size of 15.1 nm and a density of $5.6 \times 10^{11}\,\mathrm{cm}^{-2}$. However, the exact relationships between ΔV_{FB}, the size and density of the metal NCs, and E_{ox} remains unclear, and hence a quantitative analysis that considers the various factors affecting the charge storage capability of metal-NC-based NVMs is necessary.

Few researchers have attempted to explain the variables that affect the ΔV_{FB}, a measure of charge storage capability: for example, in an earlier report by Yamada *et al.*,[27] it is stated that ΔV_{FB} depends on the size and density of NCs, and that ΔV_{FB} is proportional to the total surface area of a hemispherical single NC. However, it is not enough to clearly describe the factors determining the ΔV_{FB} by considering only the size and density of NCs, owing to the variety of material systems and programming/erasing conditions, which are closely related to the tunneling probability of electrons at the tunneling oxide. Thus, the applied electric field at the tunneling oxide layer should also be considered for a quantitative analysis of ΔV_{FB}. The applied electric field at the tunneling oxide is directly related to the tunneling probability T, which can be derived from the Wentzel-Kramers-Brillouin approximation, and its time-independent approximation is as follows:[28]

$$T = \exp\left[-\frac{8\pi(2qm_{ox})^{1/2}\phi_b^{3/2}}{3hE_{ox}}\right]. \quad (2)$$

Since the tunneling probability exponentially depends on the electric field as shown in eq. (2), it can be inferred that ΔV_{FB} has a linear relationship with $\ln E_{ox}$. Figure 5 shows the experimental results of $\Delta V_{FB}/(\mathrm{NC\ density} \times \ln E_{ox})$ as a function of the surface area of the NCs. It can be seen that, considering the amount of experimental uncertainties, ΔV_{FB} per NC with respect to its surface area and the natural logarithm of the applied electric field, is in perfect match with the theoretical estimations (indicated as dashed line in Fig. 5).

To verify that our modeling can be applicable to other material systems, appropriate datasets were cited from refs. 24–26. The results using the datasets of Si, Au, and Pt NCs (open triangles and square) are placed in the bottom left corner of Fig. 5. Notably, it can be seen that the charge storage capability of a single NC studied in the previous report similarly shows a linear tendency to our proposed model, suggesting that it can be applicable to describe the charge storage capacity of individual NCs of other material systems.

The quantitative value of the stored charges in a single Pt NC can be obtained using the following equation:[29]

$$\Delta V_{FB} = \frac{qn}{\varepsilon_{ox}}\left(t_{cntl} + \frac{1}{2}\frac{\varepsilon_{ox}}{\varepsilon_{metal}}t_{NC}\right). \quad (3)$$

where q is the magnitude of an electronic charge, n is the charge density stored in NCs, ε_{metal} is the permittivity of the metal, ε_{ox} is the permittivity of SiO_2, t_{cntl} is the thickness of the control oxide layer under the gate, and t_{NC} is the diameter of NCs. In this equation, $\varepsilon_{ox}/\varepsilon_{metal}$ can be considered to be 0 since ε_{metal} is close to infinity. From the value of ΔV_{FB} at a programming voltage of 20 V, the stored charge densities were calculated to range from 1.38×10^{12} to $3.32 \times 10^{12}\,\mathrm{cm}^{-2}$, with varying mean size of the NCs from 15.1 to 55.2 nm. The numbers of stored electrons per NC were approximately 3, 14, 76, and 118, with the corresponding mean sizes of NCs of 15.1, 26.7, 47.3, and 55.2 nm, respectively.

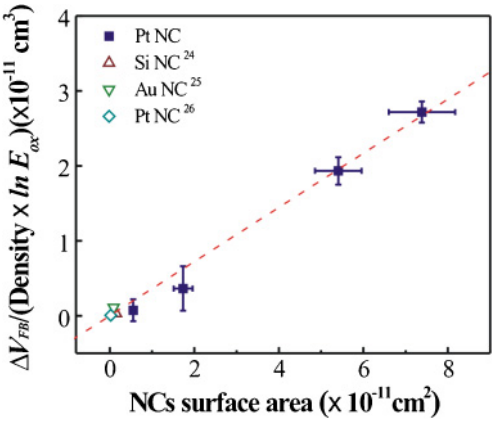

Fig. 5. (Color online) (ΔV_{FB}/NC density × ln E_{ox}) plot as a function of surface area of a hemispherical single NC. The dashed line indicates the linear fitting curve that passes through the origin. The scattered points in the bottom left corner represent the dataset taken from refs. 24–26 to comparatively analyze the charge storage capability of a single NC as a function of its surface area.

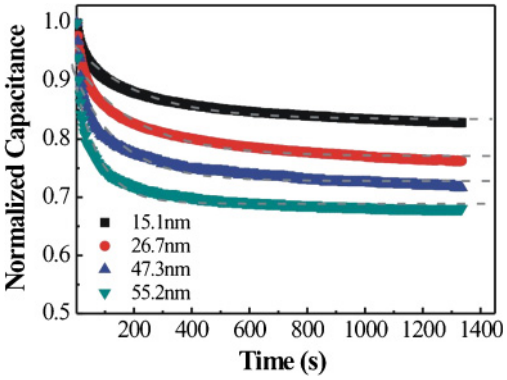

Fig. 6. (Color online) Charge retention characteristics of the NVM capacitors with varying NC size. The dashed lines indicate the exponential fitting curve.

Figure 6 shows the normalized capacitance as a function of time while varying the size of NCs, which represents the charge retention characteristics at room temperature. The programming was performed at an applied voltage of +20 V for 3 s to achieve a fully programmed state. The transient capacitance was then measured at a fixed negative bias of −1 V, which is the approximated value of V_{FB}. All the measured data were normalized using: $[C(t) - C(\mathrm{sat})]/[C(t=0) - C(\mathrm{sat})]$. The normalized capacitance decay curves obtained under our testing conditions for all the samples exhibited exponential decay as a function of time. It can be seen that the obtained curves were well fitted to the exponential decay function:

$$f(t) = \alpha \cdot \exp\left(-\frac{t}{t_0}\right) + \beta, \quad (4)$$

where α and β are constants, which are indicated as dashed lines in Fig. 6. Note that this exponential decay is composed of two decay steps; the fast-decay step and the subsequent slow-decay step. These two steps in the charge decay can be explained by two dominant mechanisms: the fast-decay step is governed by the coulomb repulsive force between the charge stored inside a single NC,[30] and the slow-decay step is governed by the stress-induced lateral leakage during the retention.[31] The charge density in a single NC has its maximum in the fully programmed state, and thus the repulsion force of individual charges should be maximized in this state, leading to a stronger electrical field that causes faster decay in the number of electrons stored in NCs. The larger the mean size of the NCs was, the steeper the decay ratio of the normalized capacitance was. As the number of charges stored in a single NC decreased, the decay ratio of stored electrons also decreases due to the weak repulsive force between the electrons. In the slow-decay step, the primary cause of the decreasing capacitance was attributed to the lateral charge leakage via the weak spots of the tunneling oxide layer. This result indicates that smaller NCs have better retention characteristics than larger ones. Compared with the values in previous reports on semiconductor-NC-based memories by Baron *et al.* (Si NC: 100 s)[10] and Ng *et al.* (Ge NC: 90 s),[32] the retention capability of the Pt-NC-based memory shown in the present report was significantly enhanced (520 s at an average NC size of 15.1 nm).

4. Conclusion

We investigated the effects of the size and density of self-assembled Pt NCs on the NVM characteristics. The size and density of Pt NCs were determined by the annealing conditions and the initial as-deposited film thickness. As the as-deposited film thickness was varied from 2 to 8 nm, the size of the NCs increased from 15.1 to 55.2 nm, and their density decreased from 5.6×10^{11} to $3.2 \times 10^{10}\,\mathrm{cm}^{-2}$. The obtained C–V measurement data showed that the large NCs had a better charge storage capability, which corresponded to a large ΔV_{FB}, while at the same time they showed a shorter retention time than the small NCs. In addition, it was shown that the charge storage capability of a single NC depended on not only the surface area of the hemispherical NCs, but also the tunneling probability of the electrons, which is determined by the applied electric field at the tunneling oxide. The theoretical model based on our experimental results showed a good agreement with previously reported memories based on metal and semiconducting (Si, Au, and Pt) NCs.

Acknowledgements

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1) R. Degraeve, B. Kaczer, and G. Groeseneken: Microelectron. Reliab. **39** (1999) 1445.
2) R. Degraeve, F. Schuler, B. Kaczer, M. Lorenzini, D. Wellekens, P. Hendrickx, M. van Duuren, G. J. M. Dormans, J. Van Houdt, L. Haspeslagh, G. Groeseneken, and G. Tempel: IEEE Trans. Electron Devices **51** (2004) 1392.
3) K. Kim: Proc. IEEE Int. Magnatics Conf., 2006, p. 102.
4) S. Park, Y. K. Cha, D. Cha, Y. Park, I. K. Yoo, J. H. Lee, K. S. Seol, and S. H. Choi: Appl. Phys. Lett. **89** (2006) 033122.
5) C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim: IEDM Tech. Dig., 2003, p. 613.
6) Y. Hu and M. H. White: Solid-State Electron. **36** (1993) 1401.
7) T. C. Chang, S. T. Yan, F. M. Yang, P. T. Liu, and S. M. Sze: Appl. Phys. Lett. **84** (2004) 4815.
8) T. C. Chang, P. T. Liu, S. T. Yan, F. M. Yang, and S. M. Sze: J. Electrochem. Soc. **152** (2005) G144.
9) S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé, and K. Chan: Appl. Phys. Lett. **68** (1996) 1377.
10) T. Baron, A. Fernandes, J. F. Damlencourt, B. De Salvo, F. Martin, F. Mazen, and S. Haukka: Appl. Phys. Lett. **82** (2003) 4151.
11) Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan: IEEE Trans. Electron Devices **49** (2002) 1606.
12) L. J. Jin and K. Dim-Lee: IEEE Trans. Electron Devices **52** (2005) 507.
13) S. K. Samanta, W. J. Yoo, G. Samudra, E. S. Tok, L. K. Bera, and N. Balasubramanian: Appl. Phys. Lett. **87** (2005) 113110.
14) S. Paul, A. Kanwal, and M. Chhowalla: Nanotechnology **17** (2006) 145.
15) D. A. Bonnell, Y. Liang, M. Wagner, D. Carroll, and M. Rühle: Acta Mater. **46** (1998) 2263.
16) T. H. Hou, C. Lee, V. Narayanan, U. Ganguly, and E. C. Kan: IEEE Trans. Electron Devices **53** (2006) 3095.
17) N. M. Park, S. H. Jeon, H. D. Yang, H. Hwang, S. J. Park, and S. H. Choi: Appl. Phys. Lett. **83** (2003) 1014.
18) B. De Salvo, G. Ghibaudo, G. Pananakakis, P. Masson, T. Baron, N. Buffet, A. Fernandes, and B. Guillaumot: IEEE Trans. Electron Devices **48** (2001) 1789.
19) T. Z. Lu, M. Alexe, R. Scholz, V. Talalaev, R. J. Zhang, and M. Zacharias: J. Appl. Phys. **100** (2006) 014310.
20) L. Perniola, B. D. Salvo, G. Ghibaudo, A. F. Para, G. Pananakakis, T. Baron, and S. Lombardo: Solid-State Electron. **47** (2003) 1637.
21) A. Geissler, M. He, J. M. Benoit, and P. Petit: J. Phys. Chem. C **114** (2010) 89.
22) M. Chhowalla, K. B. K. Teo, C. Ducati, N. L. Rupesinghe, G. A. J. Amaratunga, A. C. Ferrari, D. Roy, J. Robertson, and W. I. Milne: J. Appl. Phys. **90** (2001) 5308.
23) J. J. C. Choi, J.-S. Lee, K.-S. Min, J. Lee, D. M. Kim, and D. H. Kim: Semicond. Sci. Technol. **24** (2009) 115009.
24) Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto: J. Appl. Phys. **84** (1998) 2358.
25) C. Lee, J. Meteer, V. Narayanan, and E. C. Kan: J. Electron. Mater. **34** (2005) 1.
26) J. Dufourcq, S. Bodnar, G. Gay, D. Lafond, P. Mur, G. Molas, J. P. Nieto, L. Vandroux, L. Jodin, F. Gustavo, and T. Baron: Appl. Phys. Lett. **92** (2008) 073102.
27) K. Yamada, S. Yoshii, S. Kumagai, A. Miura, Y. Uraoka, T. Fuyuki, and I. Yamashita: Jpn. J. Appl. Phys. **46** (2007) 7549.
28) J. J. O'Dwyer: *The Theory of Electrical Conduction and Breakdown in Solid Dielectrics* (Oxford University Press, London, 1973).
29) H. I. Hanafi, S. Tiwari, and I. Khan: IEEE Trans. Electron Devices **43** (1996) 1553.
30) J. K. Kim, H. J. Cheong, Y. Kim, J. Y. Yi, H. J. Bark, S. H. Bang, and J. H. Cho: Appl. Phys. Lett. **82** (2003) 2527.
31) O. Winkler, F. Merget, M. Heuser, B. Hadam, M. Baus, B. Spangenberg, and H. Kurz: Microelectron. Eng. **61–62** (2002) 497.
32) T. H. Ng, W. K. Chim, W. K. Choi, V. Ho, L. W. Teo, A. Y. Du, and C. H. Tung: Appl. Phys. Lett. **84** (2004) 4385.