

Si/Si_{1-x}Ge_x/Si Heterojunction PIN Nanowires Fabricated by Using an Aqueous Electroless Etching Method

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(Received 29 April 2011)

The p⁺ poly-silicon/silicon-germanium/n⁺ single-crystal silicon (Si/Si_{1-x}Ge_x/Si) PIN heterojunction nanowires (NWs) were fabricated by using the aqueous electroless etching (AEE) method. The synthesized NWs were highly aligned in the vertical direction with uniform lengths of approximately 5 μm. Three distinguishable peaks of Si_{1-x}Ge_x (400), with values of x corresponding to 11.8, 16.8, and 22.2%, were clearly observed in the X-ray diffraction (XRD) pattern for the NW structures, which confirms that heterojunction NWs were successfully synthesized. Noticeably, the photo response of the photodiodes (PDs) fabricated using the heterojunction NWs was greatly increased compared to that of the bulk-based PDs. Specifically, a dramatic decrease in the dark current by three orders of magnitude was observed for the heterojunction NW-based PDs. Thus, a clear distinction of four orders of magnitude between the off-currents under the dark and light conditions was observed in the reverse bias region for the NW-based PDs whereas in bulk-based PDs the current levels differed by less than one order of magnitude.

PACS numbers: 81.07.-b, 81.07.Bc, 81.07.De

Keywords: Silicon germanium heterojunction nanowire, Aqueous electroless etching, Photodiode

DOI: 10.3938/jkps.59.501

I. INTRODUCTION

For the past few decades, silicon nanowires (SiNWs) have been extensively researched as promising candidates for potential building blocks in a variety of novel electronic devices owing to their extraordinary electrical and optical properties [1-3]. Especially, much effort has been devoted to the investigation of heterostructure semiconducting NWs based on Si to overcome the obstacles and limitations of pure Si [4-6]. Among numerous heterostructure semiconducting NWs, silicon-germanium (Si_{1-x}Ge_x) NWs have been intensively studied as they are highly advantageous in terms of higher carrier mobilities and enhanced optical detection range including the far-infrared. By convention, various methods have been developed to fabricate Si_{1-x}Ge_x NWs, including vapor-liquid-solid growth method [9], solution phase synthesis [10], and a lithography-related etching method [11]. However, the aforementioned techniques have some restrictions, as the processes generally require a high temperature or a high vacuum and the use of a template and equipment. In addition, the NWs synthe-

sized using those techniques have problems in material properties such as poor orientation, uncontrollable doping concentration, and bad alignment.

In turn, a much simpler and highly efficient process for synthesizing Si_{1-x}Ge_x NWs, the aqueous electroless etching (AEE) method, has been suggested [12]. The AEE method has been reported to be one of the most effective solution-based techniques for synthesizing Si_{1-x}Ge_x NWs in terms of simplicity in the fabrication process and feasibility of mass production of well-aligned nanowires. In addition, unlike the other methods, NWs are synthesized from the bulk material, thus, it is possible to control the doping profile of the NWs by as-doping the bulk first. Here, no additional process will be applied to induce further diffusion of dopant atoms; hence, the original doping profile will remain even after the etching process. Si_{1-x}Ge_x NWs can be readily synthesized using the AEE method, with their dimensions being controllable by varying the etching time during the synthesis process.

In this research, p⁺ poly-silicon/silicon-germanium/n⁺ single-crystal silicon (Si/Si_{1-x}Ge_x/Si) PIN heterojunction nanowires (NWs) were synthesized from the Si/Si_{1-x}Ge_x/Si PIN heterojunction bulk material by using the AEE method. The synthesized NWs were highly

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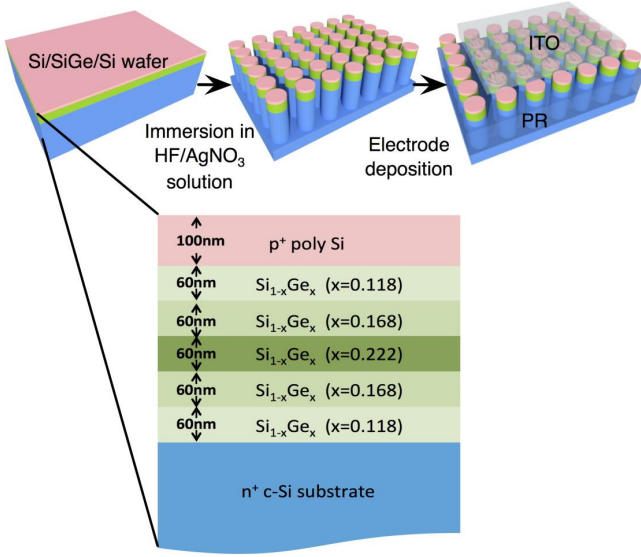


Fig. 1. (Color online) Schematic illustration of the fabrication process for obtaining the NW-based Si/Si_{1-x}Ge_x/Si PIN heterojunction PDs.

aligned in the vertical direction with uniform lengths.

An X-ray diffraction (XRD) analysis of both the bulk and the NW structures showed three distinguishable Si_{1-x}Ge_x (400) peaks, corresponding to Si_{1-x}Ge_x with 3 different x values ($x = 11.8, 16.8,$ and 22.2%), confirming that Si/Si_{1-x}Ge_x/Si PIN heterojunction NWs were successfully synthesized through the AEE method. The electrical measurement was performed after device fabrication to verify the enhanced electrical properties when compared to those of the bulk device. The measured dark current dropped from 1.0×10^{-2} A to 9.2×10^{-6} A in the reverse bias region. Thus, unlike the photo response of the bulk-based photodiode (PD) that revealed only a small difference in the dark and light current levels in the reverse bias region, a much enhanced photosensitivity could be achieved in the case of the heterojunction NW-based PD.

II. EXPERIMENTS

The epitaxial growth of 300-nm-thick graded stack layers of Si_{1-x}Ge_x (5 layers from the bottom, $x = 11.8, 16.8, 22.2, 16.8,$ and 11.8%) with 3 different Ge fractions on an n+ doped single-crystal Si (100) wafer with resistivity in the range of $0.008 - 0.02 \Omega/\text{cm}$ was carried out in an ultra-high-vacuum - chemical vapor deposition (UHV-CVD) system. The epitaxial growth of the Si_{1-x}Ge_x layers was done at 550°C in a Si₂H₆ and GeH₄ ambient. The flow rate of the Si₂H₆ gas was held constant at 10 sccm in all of the procedures, and the flow rate of the GeH₄ gas was varied from 8 to 20 sccm to control the Ge fraction over the range from 11.8% to 22.2%. Each layer was deposited to have a thickness of 60 nm. On top of the

5 grading Si_{1-x}Ge_x layers, a 100-nm-thick p-type poly Si layer with the doping concentration of $3 \pm 0.3 \times 10^{18}$ atoms/cm³ was grown through thermal CVD process at 600°C by using boron as the dopant atom. The detailed heterojunction structure is illustrated in the bottom of Fig. 1.

The native oxide removal and consequent surface termination with hydrogen (H) were carried out by dipping the Si/Si_{1-x}Ge_x/Si PIN heterojunction wafer into a 4.9-M HF aqueous solution for 5 minutes at room temperature before the AEE fabrication. The H-termination process hinders further generation of native oxide, which can interrupt the redox process between the Si surface and the highly reactive HF/AgNO₃ aqueous solution. Vertically-aligned Si/Si_{1-x}Ge_x/Si PIN heterojunction NWs were synthesized by immersing the as-prepared sample into an aqueous etching solution of 4.9-M HF mixed with 0.03-M AgNO₃ at 60°C for 10 minutes. The silver nanoparticles and other byproducts generated during the etching process were removed by dipping the sample into an HNO₃ solution for a minute. In order to carry out the electrical measurements, we deposited 150-nm-thick indium-tin-oxide (ITO) electrodes on the top surfaces of the NWs via magnetron sputtering. Prior to the deposition of the electrodes on the top surfaces, the samples were coated with a photoresist with a slight etch on the tip with O₂ plasma to firmly hold the NWs.

The surface morphologies of the Si/Si_{1-x}Ge_x/Si PIN heterojunction NWs were characterized using a JEOL JSM-600F Field-emission scanning electron microscope (FE-SEM). An X-ray diffractometer equipped with a Ni-filtered k_α ($\lambda = 1.54056 \text{ \AA}$) source was used for the structural analysis of the NWs. The current-voltage (I - V) characteristics were investigated using a Keithley 236 source-measure unit under dark and light conditions (fluorescent room light, 50 W).

III. RESULTS AND DISCUSSION

The fabrication process of the 100-nm-thick p⁺ poly-Si/300-nm-thick Si_{1-x}Ge_x/n⁺ single-crystal Si PIN heterojunction NWs is schematically illustrated in Fig. 1. The following mechanism takes place during the formation of the NWs. When the Si/Si_{1-x}Ge_x/Si PIN heterojunction structured wafer is dipped in the etching solution of HF/AgNO₃, silver nanoparticles randomly form on the surface of the wafer as a result of the galvanic displacement reaction. Silver ions have a rather high reduction potential; thus, they become reduced to metallic silver when the Si/Si_{1-x}Ge_x/Si PIN heterojunction structured wafer is simply immersed into a diluted AgNO₃ solution. Subsequently, oxidized Si and Si_{1-x}Ge_x are generated via an electrochemical redox process at the interface between the silver nano-particle (AgNP) and the wafer, which are consecutively etched with an aqueous HF solution. The chemical reaction during the etching

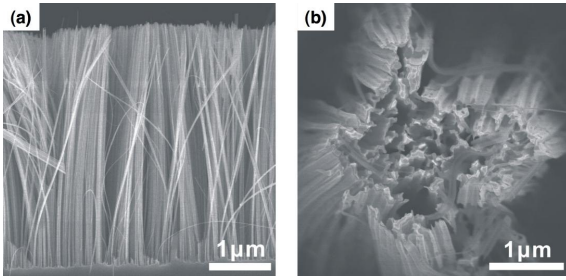


Fig. 2. SEM images of (a) top and (b) cross-sectional views of Si/Si_{1-x}Ge_x/Si PIN heterojunction NWs synthesized by immersion in a HF/AgNO₃ solution at 60 °C for 10 min.

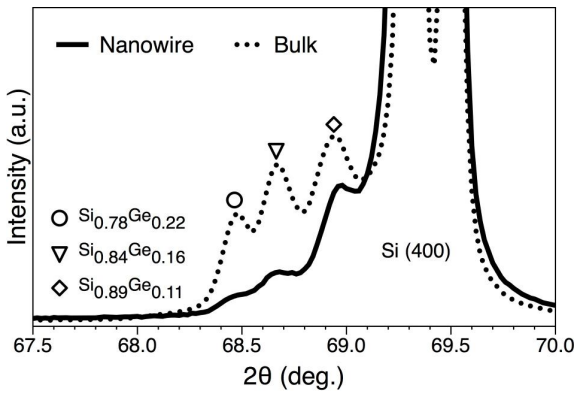
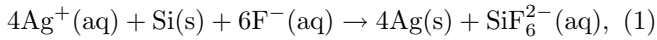


Fig. 3. XRD θ - 2θ scans from the bulk and the NW structures of the Si/Si_{1-x}Ge_x/Si PIN heterojunction.

of Si can be written as [15]



and the aforementioned process occurs in the etching of Si_{1-x}Ge_x. In the initial stage, silver ions form nuclei on the poly-Si surface. These nuclei strongly attract electrons from Si, and local oxidation occurs on the surface. Simultaneously, silicon oxide (SiO_x) is etched, and Ag-NPs make shallow pits and these process are repeated through the Si_{1-x}Ge_x. Thus continuous repetition of these sequential processes leads to the synthesis of the Si/Si_{1-x}Ge_x/Si PIN heterojunction NWs.

Figures 2(a) and (b) show typical cross-sectional and top FE-SEM micrograph images that exhibit the morphologies of the Si/Si_{1-x}Ge_x/Si PIN heterojunction NWs synthesized at 60 °C for 10 minutes, respectively. It is apparent that the synthesized NW array is perpendicular to the surface of the wafer with uniform length (~5 μm) as shown in Fig. 2(a). It should be noted that the etching profile is very uniform and is vertically oriented on a large-area scale, with the diameters of the NWs generally varying from 100 to 150 nm. In addition, the vertically-aligned NWs are bundled at their tips, as shown in Fig. 2(b). This formation of a bundle is due to the capillary force of the liquid during the drying process of the sample.

Figure 3 presents the XRD patterns of both an as-

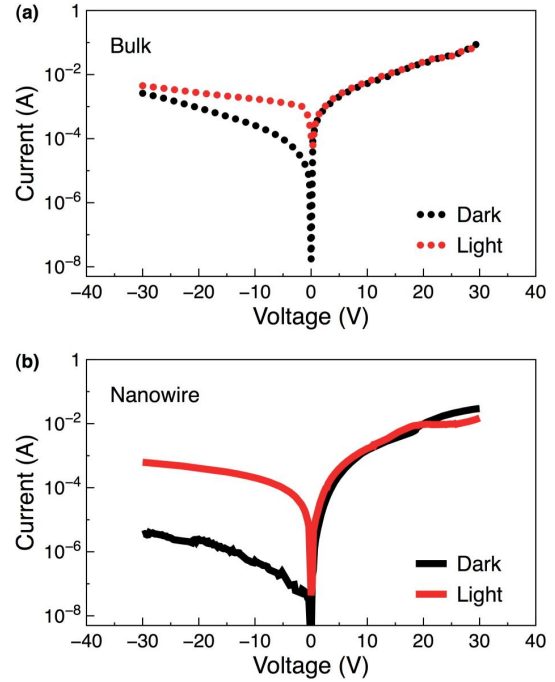


Fig. 4. (Color online) I - V characteristic curves of (a) bulk-based and (b) NW-based Si/Si_{1-x}Ge_x/Si PIN heterojunction PDs under dark and light conditions.

prepared Si/Si_{1-x}Ge_x/Si PIN heterojunction bulk and NW structure. It exhibits the Si_{1-x}Ge_x (400) peaks at 2θ values of 68.48° (for $x = 22.2\%$), 68.68° (for $x = 16.8\%$), and 68.94° (for $x = 11.8\%$), which correspond to the out-of-plane lattice constant values a_{\perp} of 5.476 Å, 5.462 Å, and 5.444 Å, respectively. This can be attributed to the strain induced at the Si_{1-x}Ge_x structure during the epitaxial film growth of Si_{1-x}Ge_x on a silicon wafer [16]. The same peaks was clearly observed after the etching process to fabricate Si/Si_{1-x}Ge_x/Si PIN heterojunction NWs. These results are quite consistent with the Vegard's rule, which is given by [17]

$$a_{\text{Si}_{1-x}\text{Ge}_x} = a_{\text{Si}} + x(a_{\text{Ge}} - a_{\text{Si}}), \quad (2)$$

where x is the Ge fraction and a is the lattice constant. If $a_{\text{Si}_{1-x}\text{Ge}_x}$ is calculated using this equation, 5.45 Å, 5.46 Å, and 5.48 Å, corresponding to $x = 11.8\%$, 16.8%, and 22.2% respectively, can be obtained which well match the measured out-of-plane lattice constants obtained from the XRD analysis. The peak intensity of the Si_{1-x}Ge_x NWs is less than that of the corresponding Si_{1-x}Ge_x films while the full width at half maximum (FWHM) intensity values, $\Gamma_{2\theta} = 0.28^\circ$, 0.36° , and 0.38° , are larger than those, $\Gamma_{2\theta} = 0.2^\circ$, 0.28° , and 0.32° , for Si_{1-x}Ge_x films, which can be attributed to the attenuated Bragg's reflection of the (400) Si_{1-x}Ge_x layers due to the gathering of the NWs at their tips.

To verify the photo response of the fabricated Si/Si_{1-x}Ge_x/Si PIN heterojunction PDs with NW and bulk structures, we measured I - V characteristic for both

NW and bulk structure devices under dark and light conditions. Figures 4(a) and (b) exhibit the I - V characteristic of the Si/Si_{1-x}Ge_x/Si PIN heterojunction PDs with bulk and NW structures, respectively. Both bulk- and NW-based devices show exponential increases in the forward bias region and good rectifying characteristics. Figure 4(a), which belongs to the photo response of the bulk-based Si/Si_{1-x}Ge_x/Si PIN heterojunction device, shows an on/off ratio of 1×10^3 and a high forward current (1.0×10^{-2} A). In the reverse bias condition, with increasing the reverse bias voltage, the difference in the off-currents slowly decreases from a two-order difference to approximately few hundreds. In the case of NW-based Si/Si_{1-x}Ge_x/Si PIN heterojunction PDs, however, a larger off-current difference was observed in the reverse bias region, and the difference was $\pm 3.23 \times 10^{-4}$, as shown in Fig. 4(b). The measured dark current of the NW-based PDs was 9.2×10^{-6} A whereas 1.0×10^{-2} A was obtained in the bulk-based PDs under the reverse bias condition, which originated from the NW structures [18].

IV. CONCLUSION

The 100-nm-thick p⁺ poly-Si/300-nm-thick Si_{1-x}Ge_x/n⁺ single-crystal Si PIN heterojunction NWs were fabricated using the facile AEE method, and ITO was deposited on top of the structures to fabricate the PDs. The synthesized NWs were highly aligned in the vertical direction and had uniform lengths. An XRD analysis was performed to confirm that the stacked layers of Si_{1-x}Ge_x remained after the etching process, and Si_{1-x}Ge_x peaks were clearly observed in the XRD patterns of both bulk and NWs structures. Enhanced electrical characteristic of the NW-based PDs, as compared to that of the bulk-based Si/Si_{1-x}Ge_x/Si PIN heterojunction PDs, were shown through photo response tests. In specific, the amount of dark current at the reverse bias region was dramatically decreased by four orders of magnitude; thus, much higher photosensitivity was achieved for the NW-based PDs, which can be attributed to the increased surface area of the NW structure as compared to that of the bulk structure. This excellent photo response of NW-based Si/Si_{1-x}Ge_x/Si PIN heterojunction PDs is applicable to far infra-red photo-detectors to detect light with a wavelength of 1.55 μm. Our approach to fabricating NW-based Si/Si_{1-x}Ge_x/Si PIN heterojunction PDs provide a simple and efficient method for device fabrication and might open a new avenue for low-dimensional semiconductor material applications.

ACKNOWLEDGMENTS

This work was supported by the Korea Aerospace Research Institute (KARI)-University Partnership program and by the IT R&D program of Ministry of Knowledge Economy (MKE)/KEIT. [10030517-2010-04, Advanced CMOS Image Sensor using 3D Integration]. This research was also supported in part by the Priority Research Centers Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2009-0093823).

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