## **RESEARCH PAPER**

# The effects of surface modification on the electrical properties of $p-n^+$ junction silicon nanowires grown by an aqueous electroless etching method

Seulah Lee · Ja Hoon Koo · Jungmok Seo · Sung-Dae Kim · Kwang Hyun Lee · Seongil Im · Young-Woon Kim · Taeyoon Lee

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Abstract Although the aqueous electroless etching (AEE) method has received significant attention for the fabrication of silicon nanowires (SiNWs) due to its simplicity and effectiveness, SiNWs grown via the AEE method have a drawback in that their surface roughness is considerably high. Thus, we fabricated surface-modified  $p-n^+$  junction SiNWs grown by AEE, wherein the surface roughness was reduced by a sequential processes of oxide growth using the rapid thermal oxidation (RTO) cycling process and oxide removal with a hydrofluoric acid solution. Highresolution transmission electron microscopy analysis confirmed that the surface roughness of the modified SiNWs was significantly decreased compared with that of the as-fabricated SiNWs. After RTO treatment, the wettability of the SiNWs had dramatically changed

S. Lee · J. H. Koo · J. Seo · T. Lee (⊠) Nanobio Device Laboratory, School of Electrical and Electronic Engineering, Yonsei University, 50 Yonsei-ro, Seodaemun-gu, Seoul 120-749, Korea e-mail: taeyoon.lee@yonsei.ac.kr

S.-D. Kim · Y.-W. Kim

In-situ Electron Microscopy Laboratory, Department of Materials Science and Engineering, Seoul University, Gwanakro 599, Dae-Hak Dong, Gwanak-Gu, Seoul 151-744, Korea

K. H. Lee · S. Im Institute of Physics and Applied Physics, Yonsei University, 50 Yonsei-ro, Seodaemun-gu, Seoul 120-749, Korea from superhydrophilic to superhydrophobic, which can be attributed to the formation of siloxane groups on the native oxide/SiNW surfaces and the effect of the nanoscale structure. Due to the enhancement in surface carrier mobility, the current density of the surface-modified  $p-n^+$  junction SiNWs was approximately 6.3-fold greater than that of the as-fabricated sample at a forward bias of 4 V. Meanwhile, the photocurrent density of the surface-modified  $p-n^+$ junction SiNWs was considerably decreased as a result of the decreases in the light absorption area, light absorption volume, and light scattering.

**Keywords** Silicon nanowire  $\cdot$  Aqueous electroless etching  $\cdot$  Rapid thermal oxidation  $\cdot$  Surface treatment  $\cdot$  $p-n^+$  junction  $\cdot$  Superhydrophobicity  $\cdot$ Nanoelectronics

# Introduction

Over the past decades, nanowires (NWs) have been extensively researched as promising candidates for potential building blocks in a variety of novel electronic devices such as transistors (Ju et al. 2005; Hong et al. 2008; Moon et al. 2010; Cui et al. 2003), photovoltaic cells (Peng and Lee 2011; Hwang et al. 2011) and sensors (Yogeswaran and Chen 2008). Many studies of the aqueous electroless etching (AEE) process for fabricating silicon nanowires (SiNWs) have been conducted, as this process is highly advantageous in terms of simplicity and its ability to produce well-aligned SiNWs with high aspect ratio in wafer-size scale (Fang et al. 2006; Peng et al. 2002, 2005, 2008; Chen et al. 2008; Jung et al. 2010; Lin et al. 2011; Ozdemir et al. 2011). Unlike other complicated NW fabrication techniques, including vapor-liquid-solid growth (Wu and Yang 2001), solution phase synthesis (Holmes et al. 2000), lithographical etching methods (Juhasz et al. 2005), laser ablation (Morales and Lieber 1998), and templateassisted growth (Lew and Redwing 2003; Kumar 2010b; Kumar et al. 2008), AEE can be used to fabricate SiNWs in a single step and may therefore be a feasible option for the mass production of lowdimensional electronic devices. Furthermore, the diameter and length of SiNWs fabricated by AEE method can be easily controlled by varying the aqueous etching solutions.

However, due to the large surface-to-volume ratio of the SiNWs, the electrical characteristics of devices based on low-dimensional materials are strongly affected by surface properties such as surface defects and dangling bonds. Specifically, SiNWs fabricated by the AEE method, despite their benefits, contain inherent surface defects that affect the electrical performance of devices fabricated from them. Thus, surface modification of the NWs is highly desirable to fabricate high-performance devices. Jie et al. sought to determine how carrier transport properties are related to the surface characteristics of AEE-grown SiNWs, and demonstrated that the performance of SiNWbased field-effect transistors can be improved by passivating the NW surface defects (Jie et al. 2008). Furthermore, SiNWs have been widely researched as photodetectors (e.g., photodiodes, photoresistors, and phototransistors) due to the fact that they have a large responsivity in the extended wavelength region of light compared to planar silicon photodetectors. Zhang et al. (2010) fabricated SiNW phototransistors that can detect both visible and infrared light due to the high density of their surface states. Kumar et al. researched the effects of the modified crystallinity and surface morphology on plasmon resonance by excimer laser and electric field, which was examined for the metal thin films (Kumar 2010a; Kumar and Krishna 2010).

In this paper, we investigated the effects of surface modification on the electrical properties of  $p-n^+$  (heavily doped *n*-type) junction SiNWs grown by the

AEE method. The surface roughness of the AEEgrown SiNWs was decreased through the sequential processes of generating silicon oxide using rapid thermal oxidation (RTO) cycling and removing the generated oxide by aqueous hydrofluoric acid (HF) etching. We verified that the surface roughness of the surface-modified SiNWs was decreased compared to that of the as-fabricated SiNWs using a transmission electron microscope (TEM). The measured current density of the RTO-treated/HF-etched SiNWs was approximately 6.3 times greater than that of the nontreated NWs at a 4 V forward bias by reduced carrier surface scattering, while the photocurrent of the SiNWs decreased due to the diminished light absorption of the modified surface.

### **Experimental details**

To obtain a planar  $p-n^+$  junction Si wafer, a 1-µmthick  $n^+$  doped layer (sheet resistance,  $R_s = 19 \ \Omega/\Box$ ) was formed on top of the 8-inch p-type (100) oriented Si (8–12  $\Omega$  cm<sup>-1</sup> and thickness of ~0.725 mm) wafer using phosphorous ion (P<sup>+</sup>) implantation (dose of  $4 \times 10^{15}$  ions/cm<sup>2</sup> at an acceleration voltage of 80 keV), followed by an activation process at 1,000 °C for 87 min (the initial implantation depth before the activation was approximately 750 nm). Native oxide removal and consequent surface termination with hydrogen (H) were accomplished by dipping the  $p-n^+$  wafer into a 4.9 M HF aqueous solution for 5 min at room temperature. The H-termination process hinders further generation of native oxide, which can interrupt the redox process between the Si wafer and the highly reactive HF/silver nitrate (AgNO<sub>3</sub>) aqueous solution.

The fabrication of the surface-modified  $p-n^+$ junction SiNWs is schematically illustrated in Fig. 1. Vertically aligned  $p-n^+$  junction SiNWs were fabricated by immersing the H-terminated samples into an aqueous etching solution of 4.9 M HF and 0.03 M AgNO<sub>3</sub> at 60 °C for various etching times ( $t_e$ ). The silver dendrites and byproducts generated in this synthesis were removed by dipping the specimens into an HNO<sub>3</sub> solution (68 wt%) for 1 min. Then, the samples were rinsed by D.I. water and dried on a hotplate at 60 °C for 30 min to remove the residual water. To modify the surface of the fabricated  $p-n^+$  junction SiNWs, surface oxidation was performed through



**Fig. 1** Schematic illustration of the fabrication process for the surface-modified  $p-n^+$  junction SiNWs

RTO at 1,000 °C for ten cycles (30 s per cycle) with an oxygen gas pressure of 100 mTorr. In each cycle, the atmosphere of the chamber was changed from  $N_2$ ambient in the ramp-up to  $O_2$  ambient during the actual annealing process, and finally to vacuum in the rapid quenching process. Then, the oxidized samples were immersed in an HF aqueous solution for 1 min to remove the thermally generated silicon oxide (SiO<sub>x</sub>), rinsed with deionized water, and left to dry in an ambient atmosphere.

For electrical measurements, 150-nm-thick indium tin oxide (ITO) electrodes were deposited via magnetron sputtering on the top surface of the  $p-n^+$  junction SiNWs using a shadow mask with circular patterns that were approximately 0.5 mm in diameter. Prior to the deposition of the ITO electrodes, the samples were coated with a nonconductive transparent photoresist (PR) material (SU-8) to isolate the SiNWs from each other. The PR was filled in the  $p-n^+$  junction SiNWs spin-coating at a speed of 3,000 rpm for 30 s. A 50-nm-thick gold (Au) layer was thermally evaporated at the bottom electrode. Subsequently, the bottom side was glued to a copper plate with a silver paste. The surface morphologies of the  $p-n^+$  junction SiNWs were characterized using a combination of a JEOL JSM-600F field emission scanning electron microscope (FESEM) and a FEI Tecnai F20 high resolution transmission electron microscope (HRTEM). An energy dispersive X-ray spectrometer equipped in the HRTEM was used for the compositional analysis of the NWs. Contact angle measurements were carried out using a Phoenix 300 equipped with a high-speed dynamic image capture system. The current–voltage (*I–V*) characteristics were investigated using a Keithley 236 source-measure unit in a probe station.

### **Results and discussion**

Figure 2a, b show typical cross-sectional and planview FESEM micrographs, respectively, illustrating the morphologies of the  $p-n^+$  junction SiNWs fabricated at  $t_e = 15$  min. It is apparent that the grown SiNW array is perpendicular to the surface of the Si wafer with uniform lengths ( $\approx 6 \,\mu m$ ) over a large area. SiNW formation can be explained through the following mechanisms. When the  $p-n^+$  junction Si wafer was dipped in the HF/AgNO<sub>3</sub> etching solution, silver nanoparticles (AgNO<sub>3</sub> was used as the catalyst) randomly formed on the surface of the wafer as a result of the galvanic displacement reaction. Subsequently, silicon oxides were generated via an electrochemical redox process at the wafer surface covered by the silver nanoparticles and etched by the HF aqueous solution. The continuous repetition of these sequential processes leads to the growth of the SiNWs (Peng et al. 2002, 2003). Figure 2c is the cross-sectional view FESEM image of the PR spin-coated SiNWs after O<sub>2</sub> plasma etching to uncover the  $n^+$  silicon tips for electrode deposition. The PR fully coated the NWs and an approximately 1- $\mu$ m-thick  $n^+$  silicon region was successfully uncovered to facilitate contact with the top ITO electrode. The barrier effects caused by the additional oxidation during  $O_2$  plasma etching could be ignored due to the low power and short duration of the O<sub>2</sub> plasma treatment. Lastly, a higher magnification SEM image of the fabricated SiNW junction diode after ITO contact formation is shown in Fig. 2d, confirming that the diameter of the grown SiNWs varied from approximately 100–150 nm.



**Fig. 2 a** Cross-sectional and **b** plan-view SEM images of the as-fabricated  $p-n^+$  junction SiNWs grown by immersing Si wafers in HF/AgNO<sub>3</sub> solution at 60 °C at  $t_e = 15$  min. **c** Cross-sectional view of the SiNWs coated with PR and treated by O<sub>2</sub>

Figure 3a is a typical TEM micrograph of individual  $p-n^+$  junction SiNWs. The contrast within a single SiNW originates from the non-uniform silicon thicknesses, indicating the rough nature of the SiNW surfaces grown by the AEE method. Using HR-TEM analysis, we observed the contrasted area at the sidewall of the as-fabricated  $p-n^+$  junction SiNW. Figure 3b shows an HR-TEM micrograph of the SiNW taken along the [011] zone axis with a corresponding fast Fourier transform (FFT) image in the inset. The roughness may be attributable to the random nature of the lateral oxidation and differential etch rate of Si atoms, which depends on their orientation in the corrosive aqueous solution during NW synthesis. These surface morphologies seen in this figure are comparable to those of the as-fabricated SiNW reported by Hochbaum et al. (2008).

plasma. The height of the exposed  $n^+$  SiNW is about 850 nm. **d** Plan-view of the fabricated SiNW diode after ITO deposition as the top electrode

Figure 3c is the HR-TEM micrograph of the RTOtreated SiNW surface, in which the thermally grown SiO<sub>x</sub> layer on the surface of the SiNWs after RTO treatment can be identified. We adopted the RTO cycling process to maximize the surface oxidation rate of the SiNWs. The thickness of the oxide increases linearly in the initial stage of oxidation. However, when the oxidation process is carried out to some extent, the oxidation rate decreases due to the formation of fixed positive charges near the SiO<sub>x</sub>/Si interface (Moslehi et al. 1985; Schafer and Lyon 1985). To reduce the generated fixed positive charges, N<sub>2</sub> gas was introduced into the chamber of the RTO system during the ramping up of the temperature in each cycle (Deal et al. 1967; Revitz et al. 1979). The thickness of the SiO<sub>x</sub> layer, as shown in Fig. 3c, is >5 nm, which is much thicker than the native oxide layer of the



**Fig. 3 a** Low-resolution and **b** high-resolution bright-field TEM micrographs of the as-fabricated  $p-n^+$  junction SiNWs (the *inset* shows the corresponding FFT image). HR-TEM

as-fabricated SiNW. We compared the as-fabricated and RTO-treated SiNWs in two respects: the interfaces between the silicon and oxide layers (hereinafter referred as "the SiNW surface"), and the outermost surfaces (the oxide surface) surrounding the SiNWs, denoted by (i) and (ii) in Fig. 3b, respectively. The interface roughness of the RTO-treated SiNWs was reduced compared to that of the as-fabricated SiNWs. Since the silicon atoms at the convex regions of the rough SiNW surface were oxidized faster than those at the concave regions, the uneven oxidation rates led to reduced interface roughness of the RTO-treated SiN-Ws. In contrast, the roughness of the outermost surface of the RTO-treated SiNWs was increased compared to that of the as-fabricated SiNWs. This increase can be attributed to the increased volume of  $SiO_x$  compared with that of Si. Figure 3d clearly shows that the

images of **c** RTO-treated and **d** RTO-treated/HF-etched SiNWs; (*i*) indicates the interface between silicon and oxide and (*ii*) is the outermost surface of the SiNWs

surface of the RTO-treated SiNWs was smoother compared to that of the as-fabricated SiNWs after the SiO<sub>x</sub> layer was etched by the HF aqueous solution. The thin oxide layer shown in the high magnification bright field TEM image (Fig. 3d) is not the thermally generated oxide, but a native oxide.

To verify the effects of RTO on the surface properties of the  $p-n^+$  junction SiNWs, the contact angles of water droplets on the as-fabricated and RTOtreated SiNWs not coated with PR were measured, as shown in Fig. 4a, b, respectively. Before measuring the contact angle on the as-fabricated SiNW, the sample was completely dried on a hot-plate at 60 °C for 30 min to remove the residual water. The contact angle measured from the optical image of a water droplet on the surface of the SiNWs fabricated at  $t_e = 25$  min and with a corresponding length of



 $\sim$  12 µm (Fig. 4a) was almost zero, indicating that the surface of the as-fabricated sample was superhydrophilic. It can therefore be concluded that the water molecules converted to hydrophilic hydroxyl ions (OH<sup>-</sup>) in the ambient air were adsorbed to the dangling bonds and surface defects of the native oxide/SiNWs (Jie et al. 2008), which are called silanol groups (-Si-O-H-). When the samples were exposed to a high concentration of oxygen gas during the RTO treatment, we found that this adsorption balance was broken. To confirm the effects of thermal treatment in  $O_2$  ambient, the same annealing process such as time and temperature of RTO treatment except the gas ambient was conducted under various ambient conditions including vacuum, nitrogen, and a mixed gas (volume ratio of  $H_2$  and  $N_2$  is 1:9). There was no significant wettability change in the surface of the SiNWs for aforementioned conditions. The contact angle was slightly increased due to the dehydration which enhances the formation of siloxane groups (-Si-O-Si) at the native oxide/SiNW surface (Nalaskowski et al. 2003). However, the surface wettability conversion from hydrophilic to hydrophobic was not occurred only after the dehydration, indicating that the formation of siloxane groups during dehydration was small and not enough to cause the wettability conversion. In our experiment, after the thermal treatment in the oxygen ambient, the contact angle was markedly increased up to 151.2° (Fig. 4b), which indicates a change in surface wettability from superhydrophilic to superhydrophobic. The investigation of oxygen chemisorption on silicon substrates by Hollinger and Himpsel indicated that siloxane groups were drastically formed on the surface of silicon substrates subsequent to annealing in the oxygen atmosphere (1983). Because the silioxane groups extremely decreased the surface energy of the oxide/SiNWs, the surface wettability was converted to hydrophobic. When the RTO-treated SiNWs were placed under ambient conditions for tens of minutes, a wettability reconversion was observed due to the re-adsorption of water molecules, which were prevalent in the air, onto the defect sites. Thus, the contact angle measurements for the RTO-treated SiNWs were performed right after RTO treatment.

In addition to the effect of adsorbed gas molecules on the surface of the SiNWs, the variable surface wettability could be due to the nanoscale structure. To investigate the surface structural effects on the change in wettability, the advancing and receding contact angles of the RTO-treated SiNWs were measured and are plotted against  $t_e$  in Fig. 4c. It is obvious that the differences between the advancing and receding contact angles were large (>21°) over the entire  $t_e$ range employed in this experiment, and this can be explained by the Wenzel state model. In this model, the large contact area which is the ratio of the actual area of liquid-solid contact to the projected area, between the liquid and the NWs enhances wettability; a hydrophobic (hydrophilic) solid becomes more hydrophobic (hydrophilic) (Quere 2008). The contact angles of water droplets on the surface of the RTOtreated SiNWs increased with  $t_e$ , and higher values of  $t_{\rm e}$  led to the growth of longer SiNWs by the AEE method (Hollinger and Himpsel 1983), which, in turn resulted in larger contact areas of the liquid and the NWs (Kuan and Chen 2009).

Figure 5a exhibits the I-V characteristics of the asfabricated, and RTO-treated/HF-etched  $p-n^+$  junction SiNWs. Both  $p-n^+$  junction SiNWs show nonlinear and good rectifying characteristics, and transport properties could be determined by the carrier mobility and carrier concentration. Of these two factors, the carrier concentration is most strongly affected by the surrounding atmosphere. Jie et al. (2008) demonstrated that the carrier concentration of the NWs could be increased due to the adsorption of molecules (especially water molecules) on the surface of the NWs. The negative charges from the aforementioned adsorbed OH<sup>-</sup> ions on the surface of the SiNWs would lead to surface band bending and produce an accumulation of excess holes in the valence band. Then, the conductance of the *p*-type SiNWs could be enhanced by the excess holes. However, when the surface depletion width by surface band bending was larger than the diameter of the NW, the recombination process was enhanced due to the reduction in surface barrier height for surface electron-hole pair recombination (Calarco et al. 2005). Such an effect may be negligible in our devices. In detail, we obtained the depletion width (W) of the  $p-n^+$  junction SiNW using the following equation (Pierret 1996):

$$W = \left[\frac{2K_{\rm S}\varepsilon_0}{q} \left(\frac{N_{\rm A} + N_{\rm D}}{N_{\rm A}N_{\rm D}}\right) (V_{\rm bi} - V)\right]^{1/2},\tag{1}$$

where  $K_{\rm S}$  is the dielectric constant of Si at 300 K,  $\varepsilon_0$  is the permittivity of free space, q is the charge on an electron,  $N_{\rm A}$  is the *p*-side doping concentration,  $N_{\rm D}$  is the *n*-side doping concentration,  $V_{\rm bi}$  is the built-in potential, and V is the applied voltage. By noting that the  $K_{\rm S} = 11.8$ ,  $N_{\rm A} = 10^{18}$ /cm<sup>3</sup>,  $N_{\rm D} = 10^{15}$ /cm<sup>3</sup>, and  $V_{\rm bi} - V = 2.67$  V, a value of  $W = 1.87 \,\mu m$  was obtained from Eq. (1). Since the estimated W is smaller than the whole length of the *p*-side SiNWs, which is  $\sim 5 \,\mu\text{m}$ , the SiNWs were not expected to be fully depleted for carriers (denoted in Fig. 5b). Furthermore, assuming that our device is not a  $p-n^+$ junction but an ITO/p-Si Schottky junction, the value of W should be much smaller than 1  $\mu$ m. Accordingly, we were able to confirm that the  $p-n^+$  junction SiNWs were successfully fabricated.

The current density enhancement of the RTOtreated/HF-etched  $p-n^+$  junction SiNWs can be ascribed to the increased surface carrier mobility. The reduced surface roughness of SiNWs treated by the sequential surface modification process corresponds to a decrease in the total number of surface defects. Consequently, the surface scattering due to the defect sites was reduced, leading to the enhanced surface carrier mobility (Hasegawa et al. 2002). In addition, in the low applied bias region, the reduced Coulomb scattering due to the eliminated surface charges may be another reason for the increased current (Cheng and Sullivan 1974). The current density of the  $p-n^+$  junction SiNWs that were modified using the RTO process for ten cycles was  $\sim$  6.3 times larger than that of the non-treated SiNWs at a 4 V forward bias. The inset of Fig. 5a shows  $ln(I/I_s)$  as a function of forward bias voltage. From the inset graph, the diode ideality factors (n) of asfabricated, and RTO-treated/HF-etched SiNWs were obtained using the following diode equation:



**Fig. 5** a Current–voltage (I-V) characteristic curves of the asfabricated and RTO-treated/HF-etched  $p-n^+$  junction SiNWs under dark conditions. The *inset* shows  $ln(I/I_s)$  as a function of forward bias at the low bias regime. **b** Perspective schematic of the fabricated  $p-n^+$  junction SiNWs

$$I = I_{\rm S} \exp\left(\frac{qV}{nkT}\right),\tag{2}$$

where I is the forward current,  $I_s$  is the reverse saturation current, k is the Boltzmann constant, and T is the absolute temperature (Fang et al. 2008). The calculated ideality factors of the as-fabricated, and RTO-treated/HF-etched samples at 300 K were 5.64 and 3.36, respectively. Both values of *n* are quite large compared to those of the conventional Si diodes due to the large surface defects caused by the high surface-tovolume ratio of NWs and the rough nature of the surface of SiNWs grown by the AEE method. The smaller n obtained from the RTO-treated/HF-etched SiNWs can be attributed to the reduced surface defects in the depletion region (Kasap 2006). In the low bias region, non-ideality is primarily dominated by the recombination process in the depletion region. In particular, since the depletion width of our  $p-n^+$ junction SiNWs was 1.87 µm, the recombination process generated in the depletion region was likely enough to affect the I-V characteristics. Thus, the decreased surface defects in the RTO-treated/HFetched sample provided fewer recombination centers for electron-hole pairs. Moreover, it was found that the current density of the SiNWs increased with increasing RTO treatment cycles (not shown here). However, the current density decreased  $\sim 0.83$ -fold at a 4 V reverse bias because the recombination-generation currents were decreased by the diminished number of surface defects available to serve as recombination-generation centers (Pierret 1996).

Figure 6 shows the photocurrent densities of the asfabricated and RTO-treated/HF-etched  $p-n^+$  junction SiNWs obtained in reverse bias. At a reverse bias of 10 V, the photocurrents of the as-fabricated and RTOtreated/HF-etched  $p-n^+$  junction SiNWs under white light illumination were 53.5 and 41.8  $\mu$ A/mm<sup>2</sup>, respectively. The reduced photocurrent of the RTOtreated/HF-etched  $p-n^+$  junction SiNWs can be explained in terms of (i) light absorption area, (ii) volume of the RTO-treated and HF-etched SiNWs, and (iii) surface geometry. The light absorption volume of the SiNWs decreased through the surface modification process, since Si atoms were consumed in the formation of SiO<sub>x</sub> layers during the RTO modification. Specifically, the radius (r) of the SiNWs decreased after the sequential surface treatment process, and this r can be related to the light absorption



**Fig. 6** Current densities of the as-fabricated and RTO-treated/ HF-etched p- $n^+$  junction SiNWs as a function of reverse voltage under white light illumination. The light was perpendicularly projected at the front side of the fabricated SiNWs. The incident optical power was 16 mW and the illuminated area of the sample was about 0.2 mm<sup>2</sup>

ability since the effective light absorbing volume decreases by  $r^2$  (volume =  $\pi r^2 h$ ). Furthermore, the flattened surface resulted in a slightly decreased surface area. In terms of surface geometry, since the smoothened surface of the RTO-treated/HF-etched SiNWs may impede the scattering of incident light, the light absorption can be suppressed. Due to the impeded light scattering, the path of the traveling light is shortened, which results in the decreased light absorption (Garnett and Yang 2010).

### Conclusion

HR-TEM images were obtained to compare the surface morphologies between as-fabricated and RTO-treated/HF-etched SiNWs, and the reduced surface roughness of the RTO-treated/HF-etched SiNWs was confirmed. Furthermore, a dramatic change in the wettability of the SiNWs from superhydrophilic to superhydrophobic was observed after the RTO treatment, which can be ascribed to the formation of siloxane groups in the native oxide/SiNW surfaces and the effect of the nanoscale structure.

The current density and photocurrent density were measured to determine the effects of surface roughness of  $p-n^+$  junction SiNWs. Due to the effects of surface roughness reduction, the forward current density of the RTO-treated/HF-etched  $p-n^+$  junction SiNWs was almost 6.3 times larger than that of the non-treated samples at 4 V, which can be attributed to enhanced surface carrier mobility. The reverse leakage current was reduced in the RTO-treated/HF-etched SiNWs compared to that in the as-grown SiNWs due to the reduced number of recombination-generation centers. In contrast, the photocurrent density of the RTO-treated/HF-etched SiNWs was considerably decreased due to the reduced light absorption area resulting from the smoothening of the SiNW surface and the reduced light absorption volume resulting from the decreased radii of the SiNWs. The presented surface-modified  $p-n^+$  junction SiNW array could be used to realize the high-performance diodes, and such method of the surface treatment using RTO can be generally applicable to enhance the performance of NW-based devices.

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