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# Selectively grown vertical silicon nanowire $p-n^+$ photodiodes via aqueous electroless etching



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Hyonik Lee<sup>a,1</sup>, Juree Hong<sup>a,1</sup>, Seulah Lee<sup>a</sup>, Sung-Dae Kim<sup>b</sup>, Young-Woon Kim<sup>b</sup>, Taeyoon Lee<sup>a,\*</sup>

<sup>a</sup> Nanobio Device Laboratory, School of Electrical and Electronic Engineering, Yonsei University, 134 Shinchon-Dong, Seodaemun-Gu, Seoul 120-749, Republic of Korea

<sup>b</sup> In-situ Electron Microscopy Laboratory, Department of Materials Science and Engineering, Seoul University, Gwanakro 599, Dae-Hak Dong, Gwanak-Gu, Seoul 151-744, Republic of Korea

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#### ABSTRACT

A facile method to selectively grow vertically-aligned silicon nanowires (SiNWs) which can inherit the doping concentration from its mother wafer, with controllable length, is demonstrated using the combination of photolithography and aqueous electroless etching. The use of SU-8-2002, a chemically and mechanically robust photoresist (PR) material, provided a high selectivity for the etching reaction on the exposed surface of 1- $\mu$ m-thick  $n^+$  doped p-type (100) Si substrate, resulting in the fabrication of ~30- $\mu$ m-long vertically-aligned SiNW photodiode arrays on the desired locations, while the areas covered with SU-8-2002 remained unreacted. Optical and field emission scanning electron microscope analyses confirmed that SiNWs were selectively grown while retaining the shape of the PR patterns. The electrical and optical measurements of the fabricated  $p-n^+$  junction SiNW photodiodes were compared to those of reference planar  $p-n^+$  junction Si photodiodes: the current density of the  $p-n^+$  junction SiNW photodiodes was approximately 3 times greater than that of the planar counterpart at the forward bias of 5 V, which can be attributed to the high density of defect states on the rough surfaces of the synthesized SiNWs, leading to the increased recombination efficiencies for the injected carriers. In addition, the photoresponse of the  $p-n^+$  SiNW photodiode arrays was 3.4 times higher than that of the planar device at -3.5 V due to the increase in the light scattering.

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### 1. Introduction

Over the past few decades, silicon nanowires (SiNWs) have been widely pursued as promising candidates for building blocks in a variety of novel electronic applications, owing to their outstanding electrical, physical, and optical properties [1–5]. Numerous techniques have been proposed for the fabrication of SiNWs, such as vapor–liquid–solid (VLS) growth [6], solution phase synthesis [7], lithography-related etching methods [8], laser ablation [9], and template-assisted growth [10]. Although the aforementioned methods are adequate for the production of laterally- or vertically-oriented NWs that have considerably high aspect ratios, these methods are still hindered by diverse challenges, including the control of the doping concentration, a hierarchical assembly, large scale synthesis, and direct integration into multi-functional

\* Corresponding author. Tel.: +82 2 2123 5767; fax: +82 2 313 2879.

*E-mail address:* taeyoon.lee@yonsei.ac.kr (T. Lee). <sup>1</sup> These authors have equally contributed to this work.

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0169-4332/\$ - see front matter © 2013 Elsevier B.V. All rights reserved. http://dx.doi.org/10.1016/j.apsusc.2013.02.099 systems. Thus, a simpler method that allows the growth of SiNWs in a single cast is highly necessary to overcome the above issues.

As a consequence, an effective solution-based, called the aqueous electroless etching (AEE) method, has been devised to fabricate SiNWs and enable the mass production of vertically-aligned SiNWs with great ease [11-14]. In addition, this method allows for control of the NW doping concentrations, since the doping profile is directly inherited from the mother Si wafer during the etching process [15]. Although Peng et al. showed that the SiNW p-njunction diode arrays could be fabricated using AEE method [16] the suggested method was not applicable for the fabrication of nanowire-embedded electronic devices. Recently, a few reports have demonstrated a method to selectively grow SiNWs using the AEE method [17,18], which would facilitate the fabrication of an integrated circuit with SiNW-based devices. In the work of Wan et al., hard mask layers such as Si<sub>3</sub>N<sub>4</sub> and SiO<sub>2</sub> were used to selectively grow SiNWs on the exposed surface of the Si substrate [17]. However, the low pressure chemical vapor deposition process for the deposition of the Si<sub>3</sub>N<sub>4</sub> and SiO<sub>2</sub> mask layers was carried out at over 600 °C, which may cause changes in the doping profile [19]. Furthermore, the maximum length of the SiNWs can be restricted to





**Fig. 1.** Schematic illustration of the fabrication process of photodiodes based on selectively grown  $p-n^+$  junction SiNWs.

the thickness of the mask layers due to the relatively poor selectivity of the hard masks in HF solution. In another report by Megouda et al., SiNWs were selectively grown on desired areas using Au mask layers with the AEE method, but their method was restricted to the use of moderately-doped Si substrates, as Au-coated Si surfaces may be etched as well when heavily-doped Si substrates are used [18].

Here, we demonstrated a facile method to selectively grow highly dense and vertically aligned SiNW arrays by using photoresist (PR) patterns as mask layers in combination with the AEE method. As a result, it is possible to achieve SiNWs with various patterns that directly replicate the shapes of the PR patterns. Notably, there were no restrictions in the length of the grown SiNWs since the PR mask layer was insoluble to the HF solution, and the doping concentration of the SiNWs remained unchanged throughout the entire process as our process did not involve any thermal processes with high temperatures. As a proof of concept, a  $p-n^+$  junction Si wafer was selectively etched to fabricate  $p-n^+$  junction SiNW photodiodes, and their electrical/optical properties were measured, and exhibited higher performances compared to those of the planar  $p-n^+$  diodes. The forward current density of  $p-n^+$  SiNW photodiode was approximately 3 times greater than that of the planar photodiode at 5V owing to the increased recombination centers by the increased surface area. The photocurrent of the  $p-n^+$  SiNW photodiode increased as much as 3.4 times compared to that of the planar device at -3.5 V as a result of the increased light absorption capabilities of the NW structures.

#### 2. Experimental

An 8-inch single-polished *p*-type  $(10 \pm 2 \Omega \text{ cm}^{-1})$  silicon wafer with (100) orientation and a thickness of ~0.725 mm was implanted with phosphorous ions ( $P^+$ ) (dose of  $4 \times 10^{15}$  ions/cm<sup>2</sup> at an acceleration voltage of 80 keV) and underwent a subsequent activation process at 1000 °C for 90 min to fabricate a planar  $p-n^+$ junction substrate with a 1- $\mu$ m-thick top  $n^+$  layer (sheet resistance,  $R_{\rm s}$  = 19  $\Omega/\Box$ ). Fig. 1 schematically illustrates the procedure to fabricate selectively grown  $p-n^+$  SiNW photodiode arrays, which was also used in our previous report of vertically-aligned SiNW synthesis [20]. In detail,  $1.5 \text{ cm} \times 1.5 \text{ cm} p - n^+$  junction Si samples were prepared and successively cleaned by ultrasonication in acetone, ethanol, and de-ionized (DI) water for 5 min each. SU-8-2002 was patterned on the cleaned samples to selectively expose the desired locations on the surface using a photo mask aligner (MDA-400 M, Midas System Co., Ltd.) equipped with a UV exposure light source with a 350W intensity controlling power supply. The samples were then immersed in an etchant composed of 4.9 M HF solution and 0.03 M AgNO<sub>3</sub> at 60 °C for 60 min. To remove the residual silver nanoparticles and byproducts generated during the etching process, the sample was immersed in a HNO<sub>3</sub> solution (68 wt%) for 1 min. Finally, the SU-8-2002 was removed through another immersion in a solution mixture of 4.9 M HF and HNO<sub>3</sub> solution (68 wt%) for a few seconds, followed by carefully rinsing with D.I water and drying at room temperature. For electrical and optical measurements, a 200-nm-thick transparent indium tin oxide (ITO) was magnetron-sputtered (DC) under a square shadow mask with the dimensions of 100  $\mu$ m × 100  $\mu$ m on the front ( $n^+$ ) side of the sample, and the entire back (p) side of the substrate was thermally evaporated with 100-nm-thick Au. Prior to the formation of the top electrode ITO contact, a negative PR (AZ 5214, Clariant Pte Ltd.) was spin-coated on the sample to isolate the SiNWs from each other and to prevent them from fracturing into pieces during the electrical measurements, and exposed with oxygen plasma at the power of 40 W for 10 min to remove the PR on the tips of the SiNWs.

The morphologies of the selectively grown  $p-n^*$  junction SiNW were observed using optical microscopy, field emission scanning electron microscope (FESEM) (JSM-6701F, JEOL Ltd.), high-resolution transmission electron microscope (HRTEM) (FEI Tecnai F20, Philips Electron Optics), and annular dark-field (ADF) scanning TEM (STEM) (FEI Tecnai F20, Philips Electron Optics). The ADF images were acquired by scanning a 3 nm probe across a specimen and recording the transmitted high-angle scattering with an annular detector (inner angle of ~44 mrad). The electrical and optical properties of the fabricated device were measured with a Kithley 236 source-measure unit under dark and light conditions (fluorescent room light, 50 W).

#### 3. Results and discussion

Fig. 2a-d shows the optical micrographs of the selectively grown  $p-n^+$  junction SiNWs with various patterns after immersion in the HF/AgNO<sub>3</sub> solution for 60 min. The patterns had rectangular shapes with dimensions of  $200 \,\mu\text{m} \times 400 \,\mu\text{m}$  (Fig. 1a) and  $200 \,\mu\text{m} \times 250 \,\mu\text{m}$  (Fig. 1b), and  $80 \,\mu\text{m}$ -thick parallel line shapes with line pitch of 130 µm (Fig. 1c), showing that SiNWs can be grown in highly defined areas that inherit their original PR pattern shapes. The patterned SiNW arrays exhibited a dark contrast, which can be attributed to the decreased reflectance and increased absorbance of light originating from the geometrical morphology of the SiNWs [21]. The slightly uneven surface observed on the exposed Si surface may have been created during the SU-8-2002 removal in the HF/HNO<sub>3</sub> solution. In general, SU-8-2002 can be removed by dissolving through a rapid thermal process in O<sub>2</sub> ambient [22]; however, immersing the sample in HF/AgNO<sub>3</sub> solution led to a chemical deformation on the surface of the SU-8-2002 [23], and it had to be stripped off by etching the surface of Si near the SU-8-2002/Si interface layer.

To illustrate the possibility of our selectively grown verticallyaligned  $p-n^+$  junction SiNW arrays for direct integration into a SiNW-containing circuit,  $p-n^+$  junction SiNW photodiode arrays consisting of repeated columns of  $3 \times 20$  rectangular patterns of SiNWs were fabricated. The dimension of a single rectangle was  $200 \,\mu\text{m} \times 400 \,\mu\text{m}$ . Fig. 3a–d shows the typical plan view and crosssectional view FE-SEM images of the selectively grown  $p-n^+$  SiNWs photodiodes prior to the top side ITO contact formation. The individual patterns of the  $p-n^+$  junction SiNW photodiode arrays had widths of 100 µm and lengths of 200 µm (Fig. 3a). Fig. 3b, a higher magnification FESEM image of the square area indicated by the white dashed-line in Fig. 3a, confirmed that the SiNWs were selectively formed in the exposed Si surface only, where their diameters were in the range of  $100 \pm 30$  nm. A further magnified FESEM image from the middle area of Fig. 3b is represented in Fig. 3c; the vertically-aligned SiNWs are bundled at their tips, which may



**Fig. 2.** Optical micrographs of the selectively fabricated p- $n^+$  junction SiNWs on the patterned Si substrate by immersing in a HF-AgNO<sub>3</sub> solution for 60 min at 60 °C; the pattern sizes are rectangles with dimensions of (a) 200  $\mu$ m × 400  $\mu$ m, (b) 200  $\mu$ m × 250  $\mu$ m, and (c) lines with widths of 80  $\mu$ m and pitches of 130  $\mu$ m.

have been induced by the capillary force of the drying liquid during the drying process of the sample after rinsing with DI water [24]. Fig. 3d exhibits the highly-ordered SiNWs grown in the vertical direction, which resulted from the use of a (100) Si substrate: the (100) plane presented two covalent bonds symmetrically directed into the reactive HF-AgNO<sub>3</sub> solution, leading to a geometry that sterically prefers etching Si atoms along the (100) direction [25]. The synthesized SiNWs were uniform in terms of their lengths of approximately 30  $\mu$ m, with marginally shorter SiNWs observed in the front row of the cross section. These NWs were mainly damaged during the sample cleavage.

Fig. 3e is a typical TEM micrograph of a single  $p-n^+$  junction SiNW: substantial bright contrasts were exhibited within the SiNW. which correspond to its thickness variation, indicating the rough nature of the SiNW surface [20]. This is a typical feature of the SiNWs synthesized using the AEE method and it could also be confirmed through the ADF STEM image in Fig. 3f. The brightness contrasts of an ADF STEM image is associated with the atomic number *Z* and thickness variation of the specimen under observation; since our specimen was a single SiNW, the dark contrasts were directly originated from the thickness variations within the SiNW. Because the SiNWs were synthesized using a solution-based etching process, faceted surfaces were naturally obtained as expected [26], which is in good agreement with the observations of our TEM and ADF STEM images. Fig. 3g shows the HRTEM micrograph of the SiNW taken along the (011) zone axis with a corresponding fast Fourier transform (FFT) image in the inset; it can be confirmed that the crystallinity of the SiNW was not destroyed through the etching process from its mother (100) Si substrate, and the dark contrast at the interface of the SiNW and  $SiO_2$  demonstrated the faceted surface roughness of the synthesized SiNW.

Compared to previous reports [17,18], the method demonstrated in our report is more readily achieved since the negative PR (SU-8-2002) is commercially available at low costs and the fabrication procedure does not include any high vacuum or high temperature processes. In addition, the SU-8-2002 was barely reacted in the HF solution, thereby providing a high selectivity for the etching reaction to affect the unmasked areas only. Consequently, a specific doping profile, inherited from its bulk structure, could be obtained, and the length of the grown SiNWs could be easily controlled by varying the etching time. The masked area is well-protected with the chemically stable SU-8-2002, and in the unmasked area of the  $p-n^+$  junction Si substrate, the following chemical reactions took place during the formation of the SiNWs using the AEE method. When the patterned  $p-n^+$  Si wafer was dipped in the etching solution HF/AgNO<sub>3</sub>, silver nanoparticles (AgNPs) were randomly formed on the unmasked surface of the substrate as a result of the galvanic displacement reactions [11]. Subsequently, Si atoms underneath the AgNPs in the unmasked Si

surface were oxidized, and were consecutively etched vertically with an aqueous HF solution. The chemical reactions during the etching of the unmasked Si can be written as follows:

$$\mathrm{Si} + 2\mathrm{H}_2\mathrm{O} \rightarrow \mathrm{SiO}_2 + 4\mathrm{H}^+ + 4e^- \tag{1}$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{2}$$

To investigate the electrical and optical properties of the fabricated  $p-n^+$  SiNW photodiode arrays, the *I–V* characteristics of the SiNW photodiode arrays were measured and compared to those of a reference planar Si photodiode. Fig. 4 shows the current densities of the selectively grown  $p-n^+$  SiNW and planar photodiodes. A nonlinear and typical diode *I–V* characteristic can be seen in the forward bias region. The threshold voltage of the selectively grown SiNW photodiode arrays was approximately 0.78 V, which is within the experimental uncertainties and thus can be regarded as the typical threshold voltage characteristic of a Si-based photodiode [27]. Notably, the current density of the planar device was higher than that of the SiNW-based device in the low forward bias region below  $\sim$ 2.2 V, which can be ascribed to the higher recombination in the depletion region at the low bias region [28]. The depletion region of the planar device was substantially larger in volume than that of the etched SiNW-base device, suggesting that the larger amounts of carrier recombination in the depletion region of the planar device contributed to the higher currents.

In the forward bias region above  $\sim$ 2.2 V, the current density of the  $p-n^+$  SiNW photodiode arrays became larger than that of the planar device, and the current density of the SiNW photodiode arrays was 3.09 times as much as that of the planar photodiodes at the forward bias of 5 V. We attribute the enlarged current to a higher dependency of the current generation in the high voltage regime on the increased number of recombination-generation centers, which originated from the surface defects of the SiNWs synthesized using the AEE method [20]. The larger quantity of carrier recombination centers is highly associated with the decrease in the minority carrier lifetimes ( $\tau_n$ ,  $\tau_p$ ), indicating that the resistance to minority carrier injection has been reduced and thus, the recombination efficiency increased. This process thereby leads to the generation of higher currents. The relationship between the minority carrier lifetimes and current density can also be explained through the diode equation, where the forward current density can be expressed as follows [29]:

$$J = J_s \exp\left(\frac{qV}{nkT}\right) \tag{3}$$

where

$$J_{\rm s} = q \left\{ \left( \frac{D_n n_{n0}}{L_n} \right) + \left( \frac{D_n p_{n0}}{L_P} \right) \right\},\tag{4}$$



**Fig. 3.** FESEM images of the fabricated  $p-n^+$  junction SiNW photodiode arrays prior to the top ITO contact formation; (a) plan view, (b) magnified image of the region indicated with a dashed rectangle in (a), and (c) magnified image of the center region of (b), and (d) cross-sectional view. (e) TEM and (f) ADF STEM micrographs of a single  $p-n^+$  junction SiNW and (g) HRTEM image of (e) on the surface.



**Fig. 4.** Current–voltage (I–V) characteristic curves of the  $p-n^+$  junction SiNW and planar Si photodiodes under dark conditions. The insets show  $I_n$   $(I/I_s)$  as a function of the forward bias at the low bias regime (right side inset) and threshold voltages (left side inset).

$$L_n^2 = D_n \times \tau_n, \text{ and}$$
<sup>(5)</sup>

$$L_p^2 = D_p \times \tau_p \tag{6}$$

Here, *J* is the forward current density,  $J_s$  is the reverse saturation current density, *q* is the electron charge, *V* is the applied voltage, *n* is the diode ideality factor, *k* is the Boltzmann constant, and *T* is the absolute temperature.  $D_n$  and  $L_n$  are the diffusion coefficient and diffusion length of the electrons in the p region, respectively, while  $D_p$  and  $L_p$  represent the diffusion coefficient and diffusion length of the holes in the n region, respectively. From Eqs. (5) and (6), it can be understood that the reduced  $\tau_n$  and  $\tau_p$  originated from the larger numbers of recombination centers contributing to the increase of the current density in the SiNW  $p-n^+$  junction diode as compared to its planar counterpart. In terms of the leakage current densities, a 3.74 times higher leakage current was obtained at -3.5 V from the  $p-n^+$  junction SiNWs diode compared to that of the planar Si photodiode, which can be explained by the same mechanism as shown in Eq. (4).

Z. Chen et al. previously reported on the electrical properties of porous Si homojunction p-n diodes [30]: a comparative analysis on the properties of our planar and NW-based  $p-n^+$  Si photodiodes with that of the porous Si p-n diodes confirmed that our results have significant validity. In particular, the diode ideality factors (n)of our  $p-n^+$  junction SiNW photodiode arrays and planar photodidoes were calculated from equation 3 and compared to that of the porous Si homojunction p-n diodes. From the inset of Fig. 3, the *n* of the SiNW-based and planar device was 5.11 and 2.70, respectively, at 300 K. For the planar Si photodiodes, the non-ideal properties were mainly associated with the carrier recombination in the depletion region [28]. The value of *n* increased notably in the case of the  $p-n^+$  junction SiNW photodiodes, owing to the increased number of surface defects that originated from the etching process. The measured *n* of the porous Si p-n photodiodes was 3 at 300 K; the porous-structured photodiodes had more surface defects than those of the planar Si photodiodes and less surface defects than those of the SiNW-based photodiodes. Thus, it seems reasonable that the diode ideality factors increased from the planar Si photodiodes to the porous p-n photodiodes, and to the  $p-n^+$  junction SiNW



**Fig. 5.** Photocurrent densities of the  $p-n^+$  junction SiNWs and planar Si photodiodes as a function of the reverse voltage under dark and light conditions.

photodiodes via the escalating number of carrier recombination centers resulting from the surface defects.

Fig. 5 shows the photoresponses of the selectively grown  $p-n^+$ SiNW and planar Si photodiodes. The measured photocurrent of the selectively grown SiNW  $p-n^+$  junction photodiodes was approximately 1.28 mA/mm<sup>2</sup> at the reverse bias of -3.5 V and that of the planar Si photodiodes was about 0.38 mA/mm<sup>2</sup>; the amount of photocurrent was increased by nearly 3.4-fold in the SiNWbased device as compared to that of the planar Si device. The increased photocurrent of the  $p-n^+$  junction SiNW photodiodes can be explained by the surface geometry of the SiNW-based photodiodes [20]. Since the roughness of the SiNW surfaces may enhance the scattering of incident light, the light absorption could have been improved. Owing to the increased light scattering, the path of the traveling light was lengthened, resulting in elevated light absorption [31].

## 4. Conclusion

In this paper,  $p-n^+$  junction SiNWs were selectively grown with the desired patterns using conventional photolithography process and the AEE method, and then were fabricated into photodiode arrays, where SU-8-2002 was adopted as a patterning mask material due to its high chemical and mechanical stability. The electrical and optical properties of SiNW  $p-n^+$  junction photodiode arrays were investigated and compared to those of a reference planar Si device with the same doping concentration; this process enhanced the measured properties of the selectively grown SiNW  $p-n^+$  junction based device compared to its planar counterpart. Due to the increased number of recombination centers originating from the inherent, abundant surface defects of the synthesized SiNWs, the recombination efficiency improved greatly improved in the  $p-n^+$ SiNW photodiode arrays, leading a current density 3 times higher than that of the planar Si photodiodes at the forward bias of 5 V. The photocurrent of the  $p-n^+$  SiNW photodiode was also 3.4 times larger compared to that of the planar device at 3.5 V, which can be primarily attributed to the increase in the light scattering of the SiNW-based photodiodes.

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#### References

- [1] S.W. Chung, J.Y. Yu, J.R. Heath, Applied Physics Letters 76 (2000) 2068-2070.
- [2] Y. Cui, C.M. Lieber, Science 291 (2001) 851.
- [3] G. Zheng, W. Lu, S. Jin, C.M. Lieber, Advanced Materials 16 (2004) 1890-1893.
- [4] L. Tsakalakos, J. Balch, J. Fronheiser, B. Korevaar, O. Sulima, J. Rand, Applied Physics Letters 91 (2007) 233117.
- [5] Y. Lee, K. Kakushima, K. Shiraishi, K. Natori, H. Iwai, Journal of Applied Physics 107 (2010), 113705-113705-113707.
- [6] Y. Wu, P. Yang, Journal of the American Chemical Society 123 (2001) 3165–3166.
- [7] J.D. Holmes, K.P. Johnston, R.C. Doty, B.A. Korgel, Science 287 (2000) 1471.
- [8] R. Juhasz, N. Elfstrom, J. Linnros, Nano Letters 5 (2005) 275-280.
- [9] A.M. Morales, C.M. Lieber, Science 279 (1998) 208.
- [10] K.K. Lew, J.M. Redwing, Journal of Crystal Growth 254 (2003) 14–22.
- [11] K.Q. Peng, Y.J. Yan, S.P. Gao, J. Zhu, Chemistry: A European Journal 6 (2000) 413.
- [12] H. Fang, Y. Wu, J. Zhao, J. Zhu, Nanotechnology 17 (2006) 3768.
   [13] K. Peng, M. Zhang, A. Lu, N.B. Wong, R. Zhang, S.T. Lee, Applied Physics Letters 90 (2007) 163123.
- [14] K. Peng, Y. Yan, S. Gao, J. Zhu, Advanced Functional Materials 13 (2003) 127–132.
- [15] J. Jie, W. Zhang, K. Peng, G. Yuan, C.S. Lee, S.T. Lee, Advanced Functional Materials
- 18 (2008) 3251–3257. [16] K.O. Peng, Y.J. Yan, S.P. Gao, J. Zhu, Advanced Materials 14 (2002) 16.

- [17] L.J. Wan, W.L. Gong, K.W. Jiang, H.L. Li, B.R. Tao, J. Zhang, Applied Surface Science 255 (2009) 3752–3758.
- [18] N. Megouda, G. Piret, E. Galopin, Y. Coffinier, T. Hadjersi, O. Elkechai, R. Boukherroub, Applied Surface Science 258 (2012) 6007–6012.
- [19] S. Banerjee, B.G. Streetman, Solid State Electronic Devices, 6th ed., PHI Learning Private Limited, New Delhi, 2009.
- [20] S. Lee, J.H. Koo, J. Seo, S.D. Kim, K.H. Lee, S. Im, Y.W. Kim, T. Lee, Journal of Nanoparticle Research 14 (2012) 1–10.
- [21] Y. Kanamori, M. Sasaki, K. Hane, Optics Letters 24 (1999) 1422-1424.
- [22] P.M. Dentinger, W.M. Clift, S.H. Goods, Microelectronic Engineering 61 (2002) 993–1000.
- [23] LJ. Yang, Y.T. Chen, S.W. Kang, Y.C. Wang, International Journal of Machine Tools and Manufacture 44 (2004) 1109–1114.
- [24] H. Lee, M.S. Kim, J. Seo, J.H. Koo, T. Lee, E.N. Cho, I. Yun, Journal of the Korean Physical Society 59 (2011) 501–504.
- [25] S. Cheng, C. Chung, H. Lee, Journal of the Electrochemical Society 155 (2008) D711.
- [26] A.I. Hochbaum, R. Chen, R.D. Delgado, W. Liang, E.C. Garnett, M. Najarian, A. Majumdar, P. Yang, Nature 451 (2008) 163–167.
- [27] R. Warner, B. Grung, Semiconductor-Device Electronics, Oxford University Press, USA, 1991.
   [28] S.O. Kasap, Principles of Electronic Materials and Devices, McGraw-Hill, New
- York, 2006.
- [29] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, Wiley-Blackwell, New York, 2007.
- [30] Z. Chen, G. Bosman, R. Ochoa, Applied Physics Letters 62 (1993) 708-710.
- [31] E. Garnett, P. Yang, Nano Letters 10 (2010) 1082-1087.