Formation of Vertically Aligned Cobalt Silicide Nanowire Arrays Through a Solid-State Reaction

Seulah Lee, Jaehong Yoon, Bonwoong Koo, Dong Hoon Shin, Ja Hoon Koo, Cheol Jin Lee, Young-Woon Kim, Hyungjun Kim, and Taeyoon Lee

***Abstract*—We report for the first time synthesis of high-density arrays of vertically well-aligned cobalt monosilicide (CoSi) nanowires (NWs) in a large area via a solid-state reaction. The vertical arrays of 1-μm-long Si NWs were first grown on a p-type (1 0 0) Si substrate by the aqueous electroless etching (AEE) method, and a 40-nm-thick Co layer was conformally deposited using a thermal atomic layer deposition system as revealed by SEM and transmission electron microscope analyses. The rapid thermal annealing process was carried out at various temperatures ranging from 700 to 1000 °C; the X-ray diffraction analysis confirmed that the polycrystalline CoSi NW arrays were formed at temperatures above 900 °C. The required high driving force for this silicide formation can be attributed to the significant amounts of oxygen-related contaminants at the defect sites of the highly rough surfaces of AEE-grown Si NWs. To demonstrate practical applications, field emitters and Schottky diodes were fabricated using the vertically aligned CoSi NW arrays. The field emission measurements showed a turn-on field of 10.9 V/μm and a field enhancement factor of 328, indicating the feasibility of vertically aligned CoSi NW arrays as promising field emitters. For the Schottky diodes, the measured Schottky barrier height was 0.52 eV and the estimated ideality factor obtained from the *I–V* characteristic curves was 2.28.**

***Index Terms*—Atomic layer deposition (ALD), cobalt silicide nanowire, field emission, rapid thermal annealing (RTA), Schottky diode, solid-state reaction.**

I. Introduction

With the aggressive scaling down of ICs, 1-D silicide nanostructures have emerged as potential candidates as fundamental components in electronic circuitry [1], [2] and as field emission emitters [3]–[5]. In particular, transition metal silicide nanowires (NWs) such as cobalt silicide [6], chrome silicide [7], iron silicide [8], nickel silicide [9], tantalum silicide [10], and titanium silicide NWs [11] have been extensively researched due to the high compatibility of their growth with silicon processing technology. Due to the advantage of the epitaxial growth of silicide NWs, many reports have demonstrated using chemical vapor deposition (CVD) for the fabrication of silicide NWs with superior electrical and magnetic properties [12], [13]. For example, Kim *et al*. reported the synthesis of high-quality single-crystalline NiSi NWs using CVD at the low temperature of ~400 °C, which exhibited typical metallic behaviors and promising field-emission properties [12]. In the report of Seo *et al*., high density free-standing single-crystalline cobalt silicide NWs with tunable compositions were grown by placing the sapphire substrates along a temperature gradient during the CVD process, and these exhibited controllable electric and magnetic properties according to the crystal structure of the NWs [13]. Another widely adopted method to fabricate silicide NWs is the solid-state reaction method, in which transition metal films are reacted with silicon NWs for silicidation [14], [15]. Using the solid-state reaction method, Lin *et al*. demonstrated the formation of novel heterostructured PtSi/Si/PtSi NWs with atomically sharp interfaces, by means of connecting the ends of the Si NW to lithographically defined Pt contact pads and subsequent annealing at 520 °C for 30 s [14]. They also reported the fabrication of high-performance nanoscale field-effect transistors that adopted metallic PtSi NWs as source and drain contacts, which exhibited excellent p-channel enhancement mode transistor behavior with a high ON/OFF ratio of $>10^7$. However, these methods can hardly offer the directional growth of silicide NWs, and the study of fabricating uniform and vertically aligned arrays of silicide NWs with high aspect ratio is essential for enhancing the field emission properties, facilitating their integration to ICs and achieving the stable performance. Especially, since the silicide NWs may have higher electric conductivity compared to semiconducting NWs, high performance of field emitter could be achievable.

Here, we demonstrate the fabrication of vertically well-aligned polycrystalline cobalt monosilicide (CoSi) NW arrays with uniform lengths of approximately 1 μm on p-type Si substrates using a combination of the aqueous electroless etching method and thermal atomic layer deposition (ALD), followed by a rapid thermal annealing (RTA) process to form silicidation of the NW arrays. The AEE method allows a facile synthesis of vertically aligned Si NW arrays as we have previously

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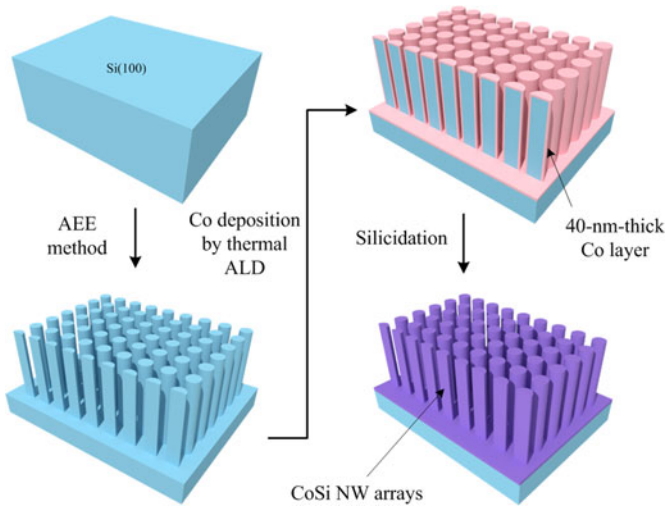

Fig. 1. Schematic fabrication procedures of vertically aligned CoSi NW arrays on p-Si substrate.

reported, and the thermal ALD of nanoscale Co films with excellent conformality and thickness controllability granted uniform capping of Si NW arrays with 40-nm-thick Co layers, which were reacted at high temperatures of above 900 °C to form CoSi. The morphologies of the vertically aligned Co/Si NW arrays before and after the RTA process were observed using a field emission scanning electron microscope (FE-SEM) and a transmission electron microscope (TEM). The composition of the CoSi NWs was confirmed through annular dark-field (ADF) scanning TEM (STEM), energy dispersive spectrometer (EDS), and X-ray diffraction (XRD) analyses. The vertically aligned CoSi NW arrays were fabricated into field emitters and diodes to examine their field emission and electrical properties, respectively. The fabricated field emitter exhibited a field enhancement factor of 328 and a turn-on field of 10.9 V/μm. Additionally, typical rectifying diode behavior was confirmed through the *I–V* characteristic curves, of which the estimated ideality factor was 2.28 and Schottky barrier height was 0.52 eV.

II. Experimental Procedures

Fig. 1 schematically illustrates the procedures used to fabricate the vertically well-aligned CoSi NW arrays on a p-type (1 0 0) oriented Si substrate with resistivity of 8–12 Ωcm^{-1}. The AEE method used in this report to obtain vertically aligned Si NWs followed procedures similar to those described in our previous reports [16], [17]: 1.2 cm $\times$ 1.2 cm samples were prepared and cleaned by successive ultrasonication in acetone, methanol, and deionized (DI) water for 5 min each, and then immersed in a 4.9 M HF aqueous solution for 5 min to remove the native oxide layer and terminate the surface with hydrogen (H). The H-termination process hinders further generation of native oxide which could interrupt the redox process between the Si wafer and the highly reactive HF/silver nitrate ($AgNO_3$) aqueous solution in the following steps. The vertically aligned SiNWs were fabricated by immersing the H-terminated samples into a solution mixture of 4.9 M HF and 0.03 M $AgNO_3$ at 60 °C for 10 min. The residual silver nanoparticles and byproducts from the etching process were removed by dipping in HNO_3 solution (68 wt%) for 1 min, followed by a thorough rinsing with DI water. The samples were then dried on a hot-plate at 60 °C for 30 min to completely remove the residual water.

The vertically aligned SiNWs were cleaned by dipping in HF for 1 min to minimize native oxide and HNO_3-induced oxide which was generated by the removal process of residual silver nanoparticles and byproducts. Then, the samples were rinsed with DI water. The 40-nm-thick Co layer was deposited on the as-prepared vertically aligned Si NW arrays using a thermal ALD chamber (Quros Plus 150) equipped with a loadlock chamber, which had a double showerhead system to ensure good uniformity. The metal-organic precursor of bis(*N,N'*-diisopropylacetamidinato) cobalt(II) (Co(iPr-AMD)$_2$) and counter reactant of NH_3 were used for the Co ALD. Co(iPr-AMD)$_2$ was contained in a stainless steel bubbler, and the temperature of the bubbler was maintained at 65 °C to obtain the suitable vapor pressure for the thermal ALD process. One ALD cycle comprised the following steps: precursor exposure t_s, purging t_p, reactant exposure t_r, and purging, for which the flow of Ar purging gas was 50 sccm. The t_s, t_r, and t_p were 6, 5, and 5 s, respectively, and the typical deposition temperature was 350 °C. Two thousand growth cycles were carried out to deposit 40-nm-thick Co film on the Si NWs, based on the growth rate of 0.2 Å/cycle. The silicidation process was carried out by annealing the specimens using an RTA system by varying the annealing temperature T_a from 700 to 1000 °C for 30 s in N_2 ambient. Prior to the annealing process, N_2 was flowed into the RTA chamber for 10 min after the sample loading to minimize the residual O_2 inside the chamber. The morphologies of the CoSi NWs arrays were characterized using a FE-SEM (JSM-6701 F, JEOL, Ltd.), an STEM ((FEI Tecnai F20, Philips Electron Optics), and a TEM (FEI Tecnai F20, Philips Electron Optics) equipped with an EDS system, which was later used for the chemical composition analysis of the as-synthesized CoSi NWs. The transition of microstructures into the silicide phase was analyzed using an XRD (Rigaku, D/Max-2500 H) system with a Cu Kα_1 source ($\lambda = 1.540562$ Å).

For the device fabrication, the cobalt oxide and residual Co from the RTA process were eliminated; the RTA-treated samples were dipped in the etching solution mixture of 95 wt% H_2SO_4 and 28 wt% H_2O_2 (4:1) at 60 °C for 20 min to remove the residual Co and cobalt oxide on the surfaces of the vertically aligned CoSi NW arrays. Field emission measurements were carried out using a planar diode configuration in a vacuum chamber at a pressure of 2×10^{-7} torr. To measure the field emission properties, the bottom of the samples were attached to a stainless steel substrate by silver paste with the cobalt silicide NWs facing upward, to form a cathode contact. The gap between the cathode and the anode was 400 μm. The emission current was monitored with a source meter unit (Keithley 2400), and the supplied voltage was managed by a dc power voltage controller (HCN140-3500). For electrical measurements, 150-nm-thick transparent indium tin oxide (ITO) electrodes were deposited via magnetron sputtering (DC) on the top surface of the CoSi NW arrays using a shadow mask with circular

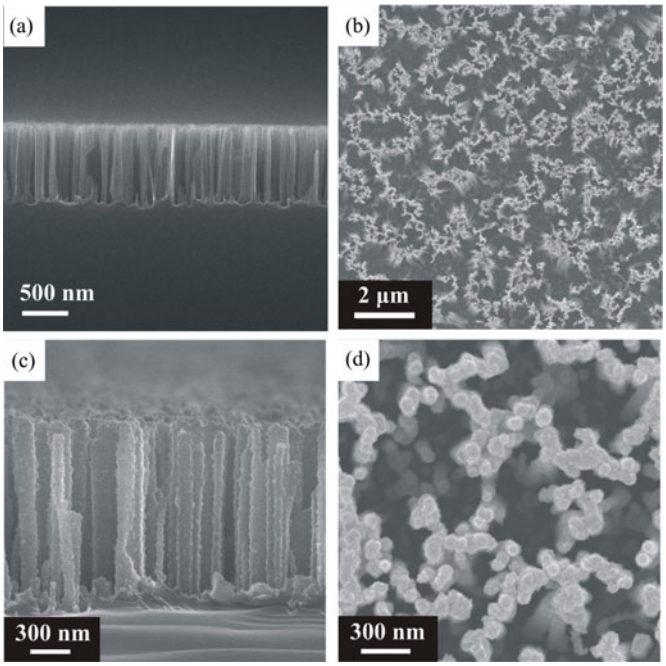

Fig. 2. (a) Cross section and (b) plan-view SEM images of the AEE-grown Si NW arrays synthesized by immersing p-Si wafers in $HF/AgNO_3$ solution mixture at 60 °C for 10 min. (c) Cross-sectional and (d) plan-view SEM images of the Si NW arrays after thermal ALD of 40-nm-thick Co.

patterns of diameter approximately of 0.5 mm. The bottom side was glued to a copper plate with a silver paste, and the *I–V* curve was measured with a Keithley 236 source-measure unit in a probe station.

III. Results and Discussion

Fig. 2(a) and (b) shows the typical cross-sectional and plan-view FESEM images of the vertically aligned p-type Si NW arrays fabricated after immersing the Si substrates in the $HF/AgNO_3$ solution for 10 min at 60 °C. The detailed mechanisms of the Si NW array formation were described in our previous reports [16], [17]: briefly, when the p-Si substrates were immersed in the etching solution of $HF/AgNO_3$, Ag nanoparticles were randomly formed on the surface of the substrates by galvanic displacement reactions. Due to the electrochemical redox process between the wafer surface and Ag nanoparticles, silicon oxides were generated at the interface of Si surface/Ag nanoparticles and vertically etched by the HF aqueous solution, which resulted in the fabrication of vertically aligned Si NW arrays. It could be observed that the Si NW arrays were well-aligned in the vertical direction, perpendicular to the substrate, with the average interspacing distance between the NWs of approximately 95 ± 5 nm [see Fig. 2(a)]. Furthermore, the lengths of the Si NWs were considerably uniform at nearly 1 μm with diameters of 150 nm, exhibiting a high aspect ratio of 10:1. The tips of the vertically aligned Si NWs were bundled [see Fig. 2(b)], which may be due to the capillary force induced during the sample drying process after rinsing with DI water [18]. Fig. 2(c) and (d) shows the cross-sectional and plan-view FE-SEM micrographs of the as-deposited Co/Si NW arrays before the silicidation. As

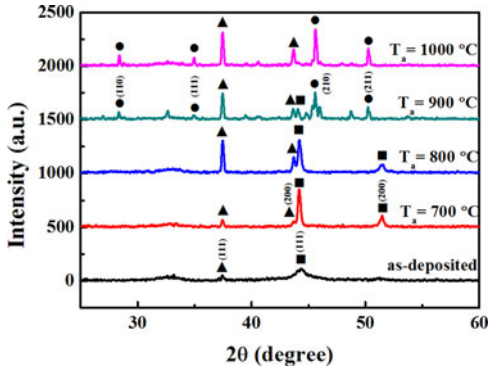

Fig. 3. ω-2θ scans of as-received Co/Si NW arrays and annealed Co/Si NW arrays at T_a = 700, 800, 900, and 1000 °C. The CoSi, CoO, and Co diffraction peaks are denoted by a closed circle (●), closed triangle (▲), and closed square (■), respectively.

shown in Fig. 2(c), the Co/Si NWs were no longer bundled at their tips after the thermal ALD of the Co layer, which indicates that the Co layer was deposited with high conformality on the surfaces of the Si NWs, with no significant variation in thickness along the lengths of the NWs. The thickness of the thermal ALD Co was 40 nm considering the interspacing distance of the Si NWs; the use of thinner Co layer (20 nm) resulted in the full-oxidation of the Co layer after the solid-state reaction, as shown in our previous report [19]. Furthermore, we did not use a Ti capping layer which is typically adopted to prevent oxygen contamination and to scavenge residual oxygen, since it may induce the formation of ternary $Co_xTi_ySi_z$ phases at high temperatures ($T_a > 850$ °C) [20], [21].

To investigate the phase transformation from Co-covered Si NWs into CoSi NWs after the RTA process, an XRD analysis was performed. Fig. 3 shows the ω-2θ scans of Co/Si NW samples before and after the RTA treatment when varying T_a from 700 to 1000 °C for 30 s in an N_2 atmosphere. In the as-deposited Co/Si NW samples, the existence of Co film on the Si NWs was confirmed by the observed β-Co (1 1 1) peak at 44.4°, whose broad shape can be ascribed to the deposited nanocrystalline Co layer using the thermal ALD [22]. In addition to the β-Co (1 1 1) peak, a CoO (1 1 1) peak was observed at 37.5°, which could have been formed during the 12-h long thermal ALD process at 350 °C. When the as-deposited Co/Si NWs were annealed at 700 °C, noticeable peaks were observed at 43.8° and 51.4°, which correspond to the peaks of Co (1 1 1) and Co (2 0 0), respectively, along with a minor peak of CoO (2 0 0) at 43.7°. When T_a was elevated to 800 °C, the intensities of Co (1 1 1) and Co (2 0 0) peaks were somewhat decreased, while those of the CoO (1 1 1) and CoO (2 0 0) were increased, which indicates that Co atoms may have been consumed to form CoO. It has been previously reported by Chevallier *et al*. that at T_a of above 750 °C, Co films were partially oxidized to form CoO [23]. The Co (1 1 1) and Co (2 0 0) peaks were further reduced as T_a was elevated to 900 °C, and they completely disappeared when T_a was 1000 °C. The formation of polycrystalline CoSi was confirmed in the samples annealed at $T_a \geq 900$ °C: the peaks at 28.4°, 34.96°, 45.61°, and 50.25° corresponded to the peaks

of CoSi (1 1 0), CoSi (1 1 1), CoSi (2 1 0), and CoSi (2 1 1), respectively.

In general, in the formation of cobalt silicides by annealing of Co thin films on Si substrates, phase transformation is known to occur in the following sequence: metal-rich silicide (Co_2Si), CoSi, and disilicide ($CoSi_2$) [24]–[26]. This can be interpreted in association with the activation energies of the cobalt silicide formation, known to be 1.5, 1.9 [24], and 2.3 eV [27] for Co_2Si, CoSi, and $CoSi_2$, respectively; higher activation energy indicates the requirement of larger driving force to form silicide phases. In the thin-film Co/Si substrate system, Freitas *et al*. reported that CoSi could be formed at 550 °C $\leq T_a \leq$ 700 °C and $CoSi_2$ at $T_a \geq$ 700 °C with the thicknesses of Co varying from 30 to 100 nm [28]. Unlike in the previous reports, however, the observed peaks in the current study indicated the formation of polycrystalline Co instead of $CoSi_2$ at 700 °C, which could be attributed to the high amounts of oxygen contamination at the defect sites of the Si NW surface, originating from the rough nature of the Si NWs grown by the AEE method [16], [29]. The AEE-grown Si NWs had highly rough surfaces, and thus the surface area of the Si NWs was significantly large; water molecules in an ambient atmosphere were prone to be physisorbed on the defect sites of the Si NW surfaces [30]. Specifically, the water molecules converted to hydrophilic hydroxyl ions (OH^-) in the ambient air, and they were adsorbed to the dangling bonds and surface defects of the native oxide/Si NWs, forming silanol groups (-Si-O-H-). Consequently, the formation of CoO at the interface of Co and Si could not be avoided during the thermal ALD of the Co layers, and the presence of native oxide on Si NW surfaces, along with the oxygen contaminants and interfacial CoO layer could hindered the diffusion and reaction of the Co atoms with Si at T_a below 900 °C, leading to the grain growth of polycrystalline Co. At T_a above 900 °C, the formation of CoSi can be attributed to the interdiffusion of Co and Si atoms at their interface with sufficient driving force, in which the diffusion of Si atoms into the polycrystalline Co layer through the grain boundaries could have been the dominant diffusion process [31].

Fig. 4(a) and (b) represents the typical TEM images of a single Co/Si NW before and after the RTA process at 1000 °C for 30 s in an N_2 atmosphere, showing that the core-shell structured Si-Co NW [see Fig. 4(a)] was transformed into well-reacted CoSi NW [see Fig. 4(b)]. This was further confirmed by the corresponding ADF STEM images [see Fig. 4(c) and (d)]: the brightness contrasts of ADF STEM images are related to the atomic numbers Z and thickness variations of the specimen under observation; in Fig. 4(c) the brighter areas in the outermost layer of the NW correspond to Co ($Z = 27$), and darker areas in the inner region correspond to Si ($Z = 14$). A considerably high surface roughness was seen in the outer layer of Co, which can be attributed to the nanocrystalline structure of the thermal ALD Co layer [22]. Further, the thickness of the outermost Co shell was approximately 40 nm, which is in good agreement with the expected value estimated from the growth rate of thermal Co ALD at 0.2 Å/cycle. In contrast to the STEM image of as-deposited Co/Si NW [see Fig. 4(c)], no significant brightness contrasts were observed in the STEM image of CoSi NW [see Fig. 4(d)], meaning that the NW was completely transformed to CoSi, which is consistent with the XRD analysis shown in Fig. 3. Due to the grain growth of polycrystalline CoSi from the reaction between nanocrystalline Co layer and Si NW, an enhanced surface roughness could be observed from Fig. 4(d). Also, the surface of the CoSi NW seems much rougher in Fig. 4(d) than in (b), since the STEM image of Fig. 4(d) was taken after the mechanical milling of CoSi NW in the sample preparation; the CoSi NW was prepared by drop-casting a CoSi NW dispersion on a Cu grid for the TEM observation in low resolution mode, instead of mechanical milling [see Fig. 4(b)]. Fig. 4(e) and (f) shows the EDS analysis of the unreacted Co/Si NW and CoSi NW, taken along the yellow lines on the STEM images of Fig. 4(c) and (d), respectively. It could be confirmed that Co was predominantly found in the outer shell of the NW with Si at the inner region [see Fig. 4(e)], while uniform distributions of Co and Si were observed after the silicidation process by RTA at 1000 °C [see Fig. 4(f)]. In Fig. 4(e), the existence of oxygen was primarily observed at the outer shell and the interface of

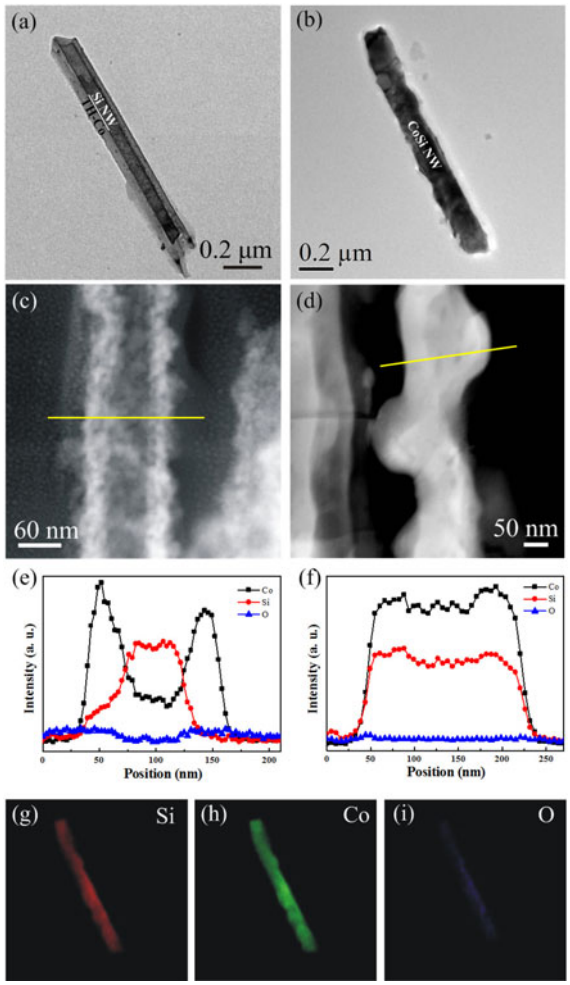

Fig. 4. Low resolution TEM micrographs of (a) as-received Co/Si NW and (b) CoSi NW after RTA at 1000 °C. (c)–(f) Corresponding STEM images and EDS analyses of (c) and (e) as-received Co/Si NW and (d), (f) CoSi NW after RTA at 1000 °C. The yellow lines in (c) and (d) indicate the actual region where the EDS analyses were performed. EDS mapping images of (g) Si, (h) Co, and (i) O atoms obtained from the CoSi NW shown in (b).

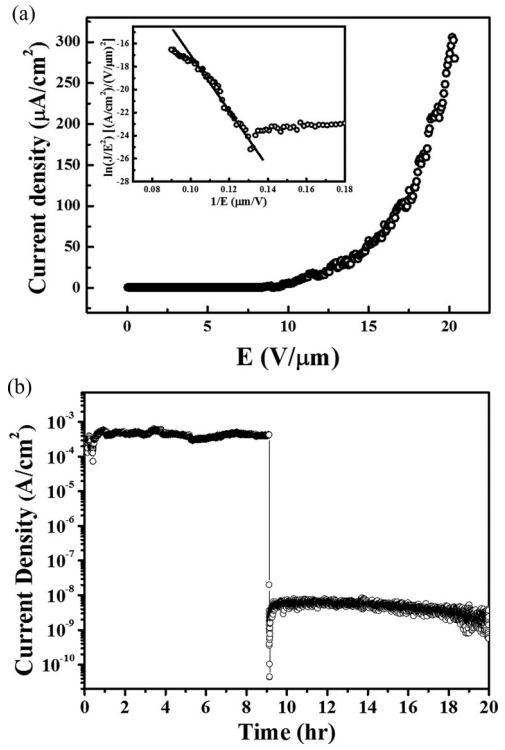

Fig. 5. (a) The field emission current density versus the applied electrical field measured in a vacuum of 2×10^{-7} torr from vertically aligned CoSi NW arrays on p-Si substrate. The inset shows the corresponding $\ln(J/E^2)$-$(1/E)$ plot. (b) The results of the stability test for the vertical CoSi NW arrays with respect to increasing time at a constant applied field of 15 V/μm.

thermal ALD Co/AEE-grown Si NW, as expected, and oxygen was observed to be evenly distributed in the CoSi NW as shown in Fig. 4(f). Finally, the EDS mapping images of the CoSi NW in Fig. 4(b) reveal that Si [see Fig. 4(g)], Co [see Fig. 4(h)], and O [see Fig. 4(i)] are homogeneously distributed within the fabricated CoSi NW, confirming that the silicidation of CoSi was uniformly achieved.

As an illustration of practical applications, the vertically aligned CoSi NW arrays synthesized at RTA of 1000 °C were fabricated into field emitters, and the corresponding field emission properties were characterized. Prior to the device fabrication, the cobalt oxides formed from unreacted Co residues were selectively removed by immersing the samples in a mixture solution of H_2SO_4 and H_2O_2 (4:1) at 60 °C for 20 min. Fig. 5(a) shows the current density J as a function of the applied electrical field (E) up to 20 V/μm. The J was calculated by the measured current divided by the cross-sectional area of NWs of which percentage is about 43% of the sample area. The turn-on field of our field emitter, which represents the value of the applied voltage to produce current density of 10 μAcm^{-2}, was 10.9 V/μm. The obtained turn-on field was relatively high compared to those of previous reports in the range of 3–8 V/μm [4], [5], [12], [32], which can be understood with the field enhancement factor, β. The field emission factor is defined as the ratio of the local electric field at the tip of an emitter, and it reflects the field enhancement ability of the emitter. The β value was calculated from the inset of Fig. 5(a), which plots the $\ln(J/E^2)$-$(1/E)$ relationship,

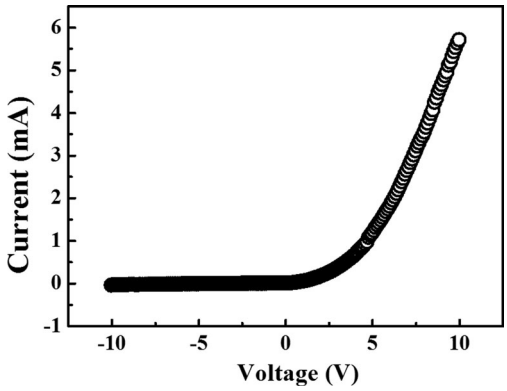

Fig. 6. Current–voltage characteristic curve of the fabricated diode structure of CoSi NW arrays/p-Si.

using the following equation that describes Fowler–Nordheim (F–N) tunneling [33]

$$J = \frac{A\beta^2 E^2}{\Phi} \exp\left(-\frac{B\Phi^{3/2}}{\beta E}\right) \tag{1}$$

where Φ is the work function of the metallic NW, and A, B are constants corresponding to 1.56×10^{-10} (A V^{-2} (eV)) and 6.83×10^3 (eV^{-3}/2 (μm^{-1})), respectively. The fitted linear relationship found in the inset of Fig. 5(a) indicates that the field-emission behavior obeys the F–N rule according to which the electrons can tunnel through the potential barrier from conduction band to vacuum state. The estimated β was approximately 328, using the work function value of 4.87 eV [34] for CoSi. Relatively higher values for β could be observed in other reports of low-dimensional silicide emitters such as $NiSi_2$ nanorods ($\beta =$ 630) [32], $TiSi_2$ NWs ($\beta = 501$) [5], NiSi NWs ($\beta = 2200$) [12], and Ti_5Si_3 NWs ($\beta = 816$) [4]. The value of β is known to be dependent on the resistivity, alignment of the NWs, and geometries of the NW tips: the fabricated metallic NW arrays in this experiment exhibited rather low resistivity due to the formation of cobalt monosilicide with polycrystalline structure, and the tips of the AEE-grown Si NWs were fairly blunt, although the NW arrays were highly aligned in the vertical direction. The β could be improved by adopting the nanosphere lithography technique in combination with the AEE method to fabricate the vertical arrays of Si NWs, by means of reducing the diameter of the NWs and changing their tip geometries [35]–[37]. Fig. 5(b) shows the current density as a function of time while applying the constant electrical field of 15 V/μm. A stable emission of current could be observed for 9 h, concluded based on observations of the small fluctuation of current density in the log scale.

Fig. 6 is the plot of *I–V* characteristic measured from the fabricated diode with a structure of vertically aligned CoSi NW arrays ($T_a = 1000$ °C) on p-Si substrate. The actual configuration of the fabricated diode structure can be found at the bottom right corner of Fig. 1. Assuming the work function of our fabricated CoSi NWs as 4.87 eV [34], a typical rectifying behavior could be expected as shown in Fig. 6. The diode ideality factor n and Schottky barrier height Φ_B of our device were estimated

using the following diode equations [38], [39]

$$I = I_s \exp\left(\frac{q\,(V - IR_s)}{nkT}\right) \tag{2}$$

$$I_S = A^* A T^2 \exp\left(-\frac{q\Phi_B}{kT}\right) \tag{3}$$

where I is the forward current, I_s is the reverse saturation current, q is the electronic charge, R_s is the series resistance, V is the applied voltage, k is the Boltzmann constant, T is the absolute temperature, A is the diode area, and A^* is the effective Richardson constant. The calculated n and Φ_B of the CoSi NW arrays/p-Si junction structure at 300 K were 2.28 and 0.52 eV, respectively. High values for n or could also be observed in other reports of heterostructured Schottky junctions such as Ge NW/Au ($n = 2.37$) [40], ZnO NW/Au ($n \sim 3$) [41], and GaN NW/Al ($n = 17.8$) [42]. The nonideality can be primarily dominated by the recombination process in the depletion region, which contains the interface of the CoSi NW arrays/p-Si substrate with presumably high-interfacial states [38]. The higher Φ_B of 0.52 eV obtained from our device compared to that from the theoretical Φ_B (0.3 eV) could be ascribed to the strong Fermi-level pinning effect [33], [38], [43]. Due to the large amounts of interfacial states between the CoSi NW arrays/p-Si substrate, which primarily originated from the formation of highly rough polycrystalline CoSi layer at the interface region of CoSi NW arrays/p-Si substrate after the RTA process, the equilibrium Fermi level was pinned within the interface band gap [44]. The interfacial states could have also affected the resistance R of the fabricated device, which can be estimated by the sum of the following series resistances R_s: contact R between the ITO and CoSi NW arrays, R of CoSi NW arrays, R of the depletion region including the interface of CoSi NW arrays/p-Si substrate, R of the bulk p-Si substrate, and the contact R between p-Si and Au back electrode. R_s was obtained using the following equation, which is the differentiated form of (2) with respect to I [39]

$$\frac{dV}{d\,(\ln I)} = n\frac{kT}{q} + IR_s. \tag{4}$$

The estimated R_s was approximately 9 kΩ, and among the aforementioned resistive parts, we mainly attribute the high R_s to the large contact area between the ITO electrode and CoSi NW arrays, along with the unetched residual CoO and interface states at the depletion region. Due to the nanostructure and high surface roughness of the fabricated CoSi NWs [see Fig. 4(d)], the contact area between the ITO and CoSi NW arrays would be substantially large, which resulted in a high contact R. In addition, the CoO may not have been totally removed after immersing the samples in a mixture solution of H_2SO_4 and H_2O_2 (4:1) at 60 °C for 20 min, and the residual oxygen-related contents could have increased R of the fabricated device.

IV. Conclusion

In summary, this paper demonstrates the fabrication of vertically well-aligned polycrystalline CoSi NW arrays using solid-state reactions of AEE-grown Si NW arrays covered with conformal Co layers at 900–1000 °C. Polycrystalline structure of CoSi were formed at high temperatures in our study, which can be understood to be caused by the significant oxygen-related contaminations at the interface of the as-synthesized Si NWs and the thermal ALD Co layers, which prevented diffusion and reactions between Co/Si atoms at temperatures below 900 °C. The formation of monosilicide NWs was probably governed by the dominant diffusion of Si atoms into the polycrystalline Co layer through its grain boundaries, which was thermally activated at the temperature range of 900–1000 °C. The uniform and vertically well-aligned CoSi NW arrays with high aspect ratio synthesized here exhibited typical rectifying behaviors and promising field-emission properties suggesting interesting strategies to fabricate silicide nanostructures which can be applicable as field emitters in Si-based microelectronics.

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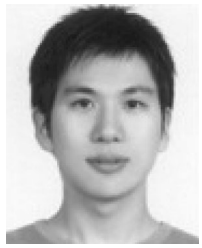

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