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## The impact of atomic layer deposited SiO<sub>2</sub> passivation for high-*k* Ta<sub>1-x</sub>Zr<sub>x</sub>O on the InP substrate†

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Metal-oxide-semiconductor (MOS) capacitors with an amorphous Ta<sub>1-x</sub>Zr<sub>x</sub>O composite gate dielectric film and a SiO<sub>2</sub> passivation layer were fabricated on an indium phosphide (InP) substrate. To investigate the impact of the passivation layer, the interfacial chemical, physical and electrical properties of the Ta<sub>1-x</sub>Zr<sub>x</sub>O/InP and Ta<sub>1-x</sub>Zr<sub>x</sub>O/SiO<sub>2</sub>/InP MOS structures were studied in detail. Electrical conductivity measurements combined with chemical bonding analysis using X-ray photoelectron spectroscopy (XPS) and electron dispersive spectroscopy (EDS) were conducted in order to evaluate the suitability of a Ta<sub>1-x</sub>Zr<sub>x</sub>O alloy as a gate dielectric film for an InP substrate. XPS results showed that the Ta<sub>1-x</sub>Zr<sub>x</sub>O film retained its insulating characteristics and was thermally stable even after annealing at 500 °C. However, Fermi-level pinning and significant diffusion of indium through the Ta<sub>1-x</sub>Zr<sub>x</sub>O were observed. The diffusion of In was remarkably reduced after introducing the SiO<sub>2</sub> passivation layer, which resulted in an overall reduction in interfacial layer thickness. Parallel conductance contour measurements showed that the SiO<sub>2</sub> passivation layer resulted in unpinning of the Fermi-level. The introduction of a SiO<sub>2</sub> passivation layer with the Ta<sub>1-x</sub>Zr<sub>x</sub>O composite gate dielectric film was found to provide remarkably improved dielectric performance, which was mainly attributed to reduced In diffusion and the passivation of interfacial and bulk dielectric defects.

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## Introduction

High-mobility III-V compound semiconductors have shown promising potential as channel materials for complementary metal-oxide-semiconductor (CMOS) logic applications due to their high electron mobility compared to Si-based devices.<sup>1</sup> However, III-V MOS devices suffer from high trap density of states ( $D_{it}$ ) at the interface that originates from Fermi-level pinning and deteriorates the electrical performance. For III-V MOS structures, the gate oxide is usually either amorphous or polycrystalline in nature and therefore a high density of dangling bonds exists at the oxide/substrate interface. High-*k* oxides have ionic bonding without a fixed coordination number which results in poor interface quality of high-*k*/III-V.<sup>2</sup> This disarray interfacial layer contains dangling bonds and broken bonds, which can cause coulomb scattering and lower the

electron mobility. Unlikely one electron dangling bond in Si-SiO<sub>2</sub>, the compensation of these dangling bonds becomes more difficult as III-V-high-*k* interfacial dangling bonds contain 0.75 electrons.<sup>2</sup> These electrically active dangling bonds form interface states in the mid-gap with different time constants resulting in Fermi-level pinning and large frequency dispersion of the capacitance. Thus, improving the metal-insulator-semiconductor (MIS) interface is a critical issue in order to successfully implement III-V channels in future CMOS circuits.

Many interface control methods have been proposed to remove or modify interfacial oxides such as atomic layer deposition (ALD) of Al<sub>2</sub>O<sub>3</sub> and ZnO, Si passivation using plasma-enhanced chemical vapor deposition (PE-CVD) and sulfur passivation.<sup>3-7</sup> III-V MOS devices with epitaxial dielectric layers having a low  $D_{it}$  have been reported.<sup>8</sup> However, the samples with the previously mentioned passivation layers showed an increase in the native oxide layer after the annealing process and did not effectively reduce interface trap density.

Recently, high dielectric constant (*k*) materials have received attention as a candidate for the replacement of SiO<sub>2</sub> because future generation CMOS devices require an equivalent oxide thickness (EOT) of less than 1 nm with a very low gate leakage current.<sup>9,10</sup>

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Among the reported candidates, Ta<sub>2</sub>O<sub>5</sub> has attracted a lot of attention due to its high dielectric constant.<sup>11,12</sup> However, the use of Ta<sub>2</sub>O<sub>5</sub> has technical challenges related to its thermal stability and defects induced by oxygen vacancies. Specifically, when Ta<sub>2</sub>O<sub>5</sub> is in contact with a semiconductor, it forms a defective interfacial layer with poor electrical properties at an elevated annealing temperature.<sup>13</sup> In addition, Ta<sub>2</sub>O<sub>5</sub> has a small band gap resulting in a band offset at the Ta<sub>2</sub>O<sub>5</sub>-semiconductor interface.<sup>14</sup> Interestingly, Ta<sub>2</sub>O<sub>5</sub> films doped with Hf, Al, or Zr showed significant improvement in the physical and electrical properties such as the crystallization temperature, thermodynamic stability of the interface layer, effective dielectric constant ( $k_{\text{eff}}$ ), dielectric breakdown strength and leakage current density because the dopant ions compensated for oxygen vacancies.<sup>15–20</sup> Lu and Paskaleva *et al.* reported that Hf could easily intermix with Ta<sub>2</sub>O<sub>5</sub> and the mixed Hf-Ta<sub>2</sub>O<sub>5</sub> layer had a wider energy band gap than the undoped Ta<sub>2</sub>O<sub>5</sub>.<sup>15,16</sup> According to Tewg *et al.*, improved electrical properties resulting in a small flatband voltage shift and low hysteresis were achieved by carefully adjusting the Zr dopant concentration in lightly Zr-doped Ta<sub>2</sub>O<sub>5</sub> films.<sup>18</sup> In this strategy, Zr acted as an acceptor and effectively compensated for the oxygen vacancies in Ta<sub>2</sub>O<sub>5</sub> resulting in reduced leakage current. In some previous studies it was reported that, indium can be diffused through high- $k$  by thermal induction or post deposition annealing and degrades the device performance. Krylov *et al.* correlated the occurrence of out-diffused indium in the high- $k$  dielectric layer with the increase of gate leakage current.<sup>21</sup> Recently In diffusion and the formation of P-oxide in HfO<sub>2</sub> high- $k$  dielectrics has been reported by An *et al.* and Kang *et al.* by different chemical analyses.<sup>22,23</sup> In and P rich interface always leads to high interface trap density. So it is highly desirable to reduce the substrate out-diffusion process to achieve good interface quality. Also a detailed analysis of substrate elemental diffusion need to be addressed during thermal annealing.

In recent studies Dalapati *et al.* and Lee *et al.* worked with ALD SiO<sub>2</sub> and liquid-phase-deposited (LPD) SiO<sub>2</sub> on GaAs respectively.<sup>24,25</sup> In their study they used only SiO<sub>2</sub> dielectric on the GaAs substrate without applying any high- $k$  dielectrics. According to Dalapati *et al.* upon thermal annealing SiO<sub>2</sub> makes improved interface quality and reduces  $D_{\text{it}}$ . On the other hand Lee *et al.* in their study showed that 10 nm SiO<sub>2</sub> along with a 1.5 nm Si interface passivation layer on GaAs can improve electrical performance by reducing native oxide growth. So we attempted for the first time an ALD-SiO<sub>2</sub> passivation layer along with high- $k$  dielectric Ta<sub>1-x</sub>Zr<sub>x</sub>O on InP.

In this paper, we improved the III-V MOS capacitor properties by simultaneously adopting two methods. The first method was the incorporation of Zr into the Ta<sub>2</sub>O<sub>5</sub> dielectric to suppress the formation of oxygen vacancies, resulting in an increase in the overall capacitance and dielectric constant. In the second method, we introduced an ALD SiO<sub>2</sub> interfacial layer to control the interfacial layer growth and minimize  $D_{\text{it}}$ . Measurements of the interface defect densities and the electrical activity of the defects were obtained under different processing conditions. We observed that a thin ALD SiO<sub>2</sub> layer at the interface between

the high- $k$  Ta<sub>1-x</sub>Zr<sub>x</sub>O layer and the InP substrate can effectively reduce interface traps, substrate element diffusion and can minimize the frequency dispersion of the capacitance.

## Results and discussion

Fig. 1(a) shows a cross section High Resolution Transmission Electron Microscopy (HR-TEM) image of the interface between Ta<sub>1-x</sub>Zr<sub>x</sub>O and InP. The TEM image confirms the presence of a thick interfacial layer between the Ta<sub>1-x</sub>Zr<sub>x</sub>O and the InP substrate after ALD. As shown in Fig. 1(a), the 9.2 nm thick gate stack actually consists of a 6.5 nm thick layer of Ta<sub>1-x</sub>Zr<sub>x</sub>O and a 2.7 nm thick interfacial layer. EDS mapping of the same sample shows the elemental Ta, Zr and In distribution in the cross section. As shown, Ta and Zr are uniformly distributed throughout the dielectric layer, as indicated by the blue and green data points (TaL $\alpha$  [●], ZrK $\alpha$  [●]). The EDS image also shows that In diffusion cannot be controlled using only Zr

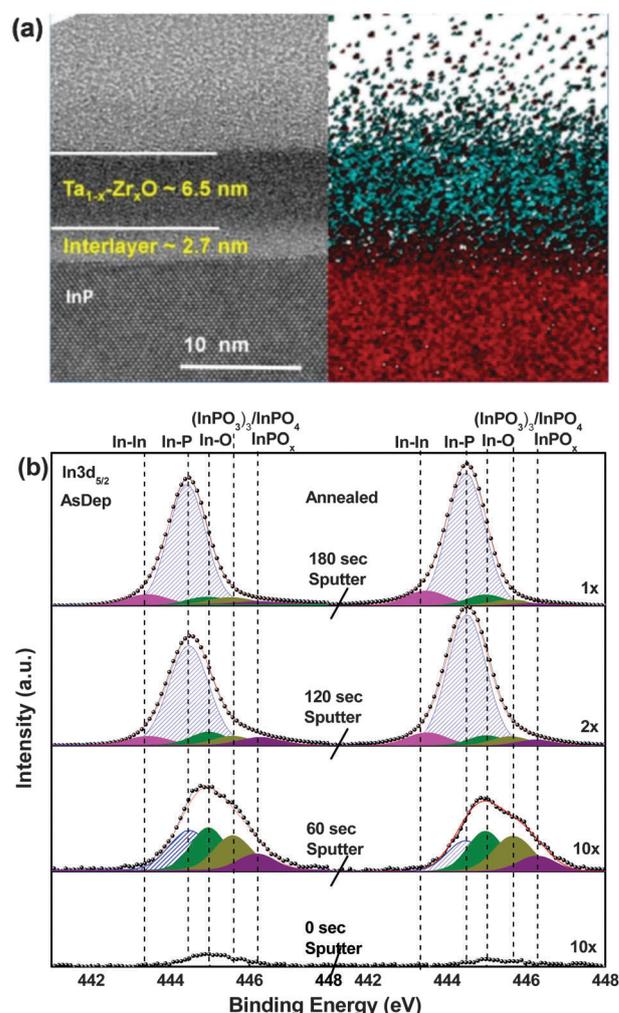


Fig. 1 (a) Cross-sectional TEM micrographs and EDX elemental analysis (TaL $\alpha$  [●], ZrK $\alpha$  [●] and InL $\alpha$  [●]) for Ta<sub>1-x</sub>Zr<sub>x</sub>O on InP. XPS core level spectra of In3d<sub>5/2</sub> for (b) as-deposited and annealed samples at different Ar<sup>+</sup> sputtering times.

incorporation into Ta<sub>2</sub>O<sub>5</sub>, as indicated by the red data (InLα [●]) in Fig. 1(a). To investigate the chemical composition of the interfacial layer, the In 3d<sub>5/2</sub> core level XPS spectra of the films were obtained at various Ar<sup>+</sup> sputtering times. Fig. 1(b) shows the XPS spectra of the Ta<sub>1-x</sub>Zr<sub>x</sub>O/InP interface with sputtering times from 0–180 s. During XPS peak fitting, an accurate deconvolution of the whole spectra was difficult due to the low intensity of some peaks and the relatively small binding energy separation between the metallic In3d bulk peak and various In- and P-related mixed oxidation states. However, the main contributing oxidation states were fitted for ‘as-deposited’ and ‘annealed’ samples. These results are consistent with recent observations for high-*k*/InP and they suggest that diffusion is common in high-*k*/III-V MOS devices that have unstable high-*k*/InP interfaces.<sup>26</sup>

In addition to the bulk Ta<sub>1-x</sub>Zr<sub>x</sub>O dielectric layers, we systematically examined interfacial layers of Ta<sub>1-x</sub>Zr<sub>x</sub>O/InP using different Ar<sup>+</sup> sputtering times between 0–180 s. The In3d core level spectra showed In–O (likely In<sub>2</sub>O<sub>3</sub>) peaks, which are a combination of In(PO<sub>3</sub>)<sub>3</sub>/InPO<sub>4</sub> and InPO<sub>x</sub>. The reference value of the binding energy for In3d<sub>5/2</sub> (In–P) was taken to be 444.5 eV. A peak with a binding energy separation of Δ ~ 0.5 eV with respect to the InP bulk peak was assigned to In–O (In<sub>2</sub>O<sub>3</sub>). The contribution from In–S bonding on the (NH<sub>4</sub>)<sub>2</sub>S treated samples was found to be very small and was therefore neglected. A peak with a binding energy separation of Δ ~ 1.1 eV with respect to the InP bulk peak was assigned to a state with a mixture of In and P oxides, likely a mixture of InPO<sub>4</sub>/In(PO<sub>3</sub>)<sub>3</sub>.<sup>27,28</sup> Based on a previous work, the peak associated with a binding separation of Δ ~ 1.7 eV was identified as InPO<sub>x</sub>.<sup>29</sup> Due to the sensitivity of the detection limit of the XPS above 5–6 nm thickness of high-*k* dielectrics, it was needed to sputter the surface for possible detection of the desired signal above the noise level. There was no significant emission of electrons and barely could get any peak under 0–60 s. After 60 s of sputtering, XPS fitting showed that the metallic In content was very low and In/P related oxides dominated. This region was the interface between the high-*k* Ta<sub>1-x</sub>Zr<sub>x</sub>O and oxide interfacial layers. Furthermore, this region seemed to be quite thick since 60 s of Ar<sup>+</sup> sputtering was not enough to observe the In–P substrate peak. Additional sputtering revealed a region (for sputtering times between 120 to 180 s) with notable metallic In content, which was attributed to the interface between the In/P-oxide and the InP substrate. This interface layer may have formed due to the diffusion of In or P ions into the dielectric and subsequent oxidation during high temperature ALD. After annealing at 500 °C, there was no notable increase in interfacial oxidation, as shown in Fig. 1(b). The binding energy separations between In–P and In–oxide were similar before and after N<sub>2</sub> annealing, which suggests that the In–oxide chemical state did not change after high temperature annealing. Also, the In–O area after annealing remained approximately the same as that found from the XPS scans after sputtering for 0–180 s; this result suggests that In–O diffused into Ta<sub>1-x</sub>Zr<sub>x</sub>O and was close to the surface regardless of annealing.<sup>30</sup> So, we confirmed that the thermodynamic stability of the interfacial layer after Zr incorporation into Ta<sub>2</sub>O<sub>5</sub> remained unchanged after high temperature annealing.

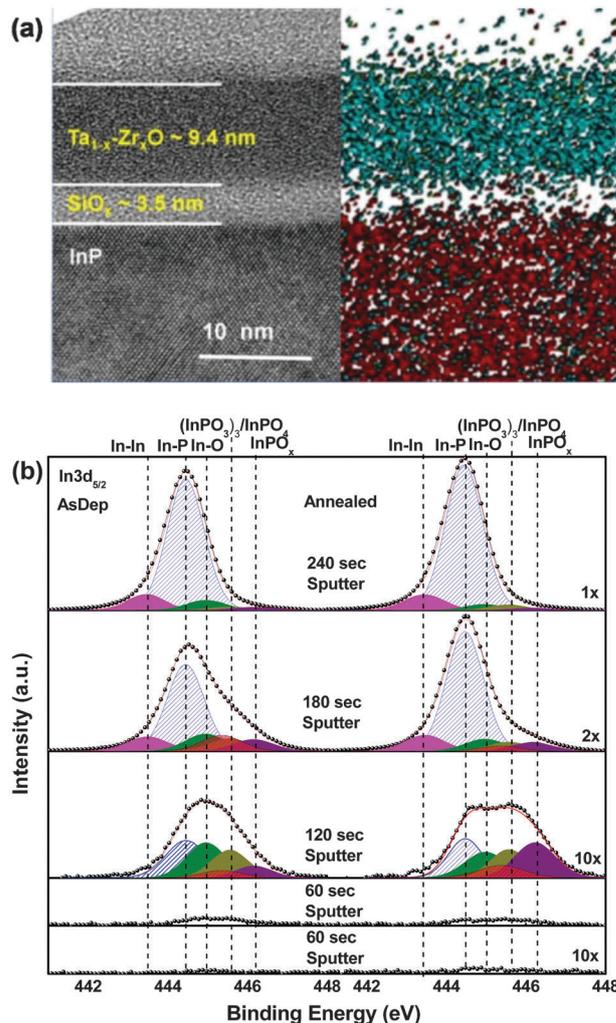


Fig. 2 (a) Cross-sectional TEM micrographs and EDX elemental analysis (TaLα [●], ZrKα [●] and InLα [●]) for Ta<sub>1-x</sub>Zr<sub>x</sub>O/SiO<sub>2</sub> on InP. XPS core level spectra of In3d<sub>5/2</sub> for (b) as-deposited and annealed samples at different Ar<sup>+</sup> sputtering times.

The interface between Ta<sub>1-x</sub>Zr<sub>x</sub>O and the InP substrate was investigated after ALD SiO<sub>2</sub> passivation using TEM, EDS and XPS, as shown in Fig. 2(a and b). Comparing the TEM images and EDS analyses in Fig. 1(a) and 2(a), we observed that, after ALD SiO<sub>2</sub> passivation, the upper Ta<sub>1-x</sub>Zr<sub>x</sub>O layer retained its thickness and the interlayer (IL) thickness decreased significantly. The reduction in the IL thickness might be because Si can form strong covalent bonds with oxygen, while In or P bonds with oxygen are relatively weaker. Therefore, during annealing in a N<sub>2</sub> atmosphere, the oxygen atoms of the IL diffused into the vacancies in the SiO<sub>2</sub> layer and reacted with Si. As a result, the IL became thinner, thereby decreasing interfacial layer growth. Although a detailed discussion of the presence of sub-oxide components is difficult because of the limited energy resolution and weak XPS intensity, the data suggested that In–O related sub-oxides were present.

Different forms of partial silicate formation upon high-*k* deposition on amorphous-Si/InP were previously reported by

Dong *et al.*<sup>6</sup> Specifically, they noted that the presence of a P–P/Si bond or In–In/Si at the interface upon additional thermal annealing can likely form partial Al- or Hf-silicate along with  $\text{SiO}_x$  due to a lack of oxygen. However, in this present study we observed partial silicate formation along with  $\text{SiO}_2$  after introduction of a  $\text{SiO}_2$  interfacial layer by ALD. This observation was confirmed by the increased width of the  $\text{In}3d_{5/2}$  spectra. Specifically, we found that In–O–P bonds located at the InP substrate were easily converted to Si–O–In/P bonds during high temperature ALD deposition and annealing. Similar oxidation mechanisms were described in earlier reports for the interaction of different metals with the InP substrate.<sup>31</sup> Narrow scan spectra of the In  $3d_{5/2}$  core level of the  $\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{SiO}_2/\text{InP}$  sample are shown in Fig. 2(b). Similar to the  $\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{InP}$  interface, in this case we deconvoluted the  $\text{In}3d_{5/2}$  spectra into peaks characteristic of  $\text{In}_2\text{O}_3$ ,  $\text{In}(\text{PO}_3)_3/\text{InPO}_4$  and  $\text{InPO}_x$ . Additionally, the low intensity peak (red with line pattered) at a binding energy separation of  $\Delta \sim 0.9$  eV with respect to the InP bulk peak was assigned to In/P–O–Si due to the formation of silicate. This silicate-related peak was also found after annealing, as seen in Fig. 2(b). Increasing intensity of  $\text{InPO}_x$  appearing after annealing can also be related to silicate formation. Though it is unclear at this time. Silicate formation depended on the diffusion of both Si and oxygen and can be understood as a temperature dependent process similar to the well-known silicon oxidation process. Thus, the In/P–O–Si fitted peak intensity increased with increasing silicate layer thickness. This suggests that some additional oxidation took place at the IL/ $\text{SiO}_2$  interface during  $\text{N}_2$  annealing resulting in the creation of Si–O bonds. The source of the oxygen was either residual oxygen in the annealing chamber or oxygen extracted from the IL during the  $\text{SiO}_2$  deposition process. After  $\text{Ar}^+$  sputtering for 180–240 s, the InP substrate surface was exposed and the In–P peak became dominant. The fits of the  $\text{In}3d_{5/2}$  data for the as-deposited and annealed samples after sputtering for 180 and 240 s were similar. This implies that the interface layer growth did not change within a few angstroms of the InP surface upon annealing of the  $\text{SiO}_2$  passivated samples.

To further confirm the formation of silicate,  $\text{Si}2p$  XPS spectra were measured (Fig. 3) and these data confirmed the presence of Si and Si–O bonding in the IL before annealing. A previous work has shown that the peak with a binding energy at around 99.6 eV and 100.2 is directly related to the signal of  $\text{Si}^0 2p_{3/2}$  and  $\text{Si}^0 2p_{1/2}$  spectra from metallic silicon and the binding energy at approximately 103.5 eV is believed to be due to fully oxidized  $\text{SiO}_2$ .<sup>32</sup> After annealing of the sample at 500 °C under  $\text{N}_2$ , the extra silicate peak shifted to  $\sim 102.8$  eV, which was slightly lower than the main silicate peak. This is likely due to the high temperature annealing process, which may have increased the oxygen content in the silicate layer or increased the thickness of the silicate layer. In any case, we concluded that the XPS results show that the stoichiometry of a pre-grown In/P-oxide layer can be changed by a subsequent ALD  $\text{SiO}_2$  deposition and a thermal annealing process. This strategy provides better control of the IL, which is valuable in the formation of high- $k$  gate dielectrics.

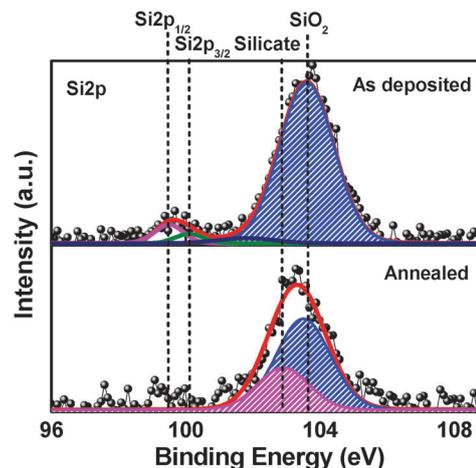


Fig. 3  $\text{Si}2p$  spectra at the interface of  $\text{SiO}_2/\text{InP}$  for as-deposited samples and samples annealed at 500 °C in an ambient  $\text{N}_2$ .

To understand the interfacial oxidation states in more detail we also have analyzed the  $\text{P}2p$  core level spectra along with the  $\text{In}3d_{5/2}$  and  $\text{Si}2p$  core level. Fig. 4 shows the oxide and bulk component in the  $\text{P}2p$  spectrum for the  $\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{InP}$  interface with and without  $\text{SiO}_2$  passivation under different sputtering conditions. In Fig. 4 before 60 s sputtering P-diffusion related peaks for both as-deposited and annealed conditions are found close to the detection limit of XPS. After 60 s sputtering conditions the  $\text{P}2p$  spin–orbit splitting was evident from peak asymmetry and the spectrum was fitted with a  $\text{P}2p_{3/2} : \text{P}2p_{1/2}$  intensity ratio of 2, with a spin–orbit splitting of 1 eV.<sup>33</sup> The binding energy of 128.5 was taken as the reference for  $\text{P}2p_{3/2}$  which was in good agreement with the reported results of the literature.<sup>34</sup> The oxide related peak with a binding energy separation of

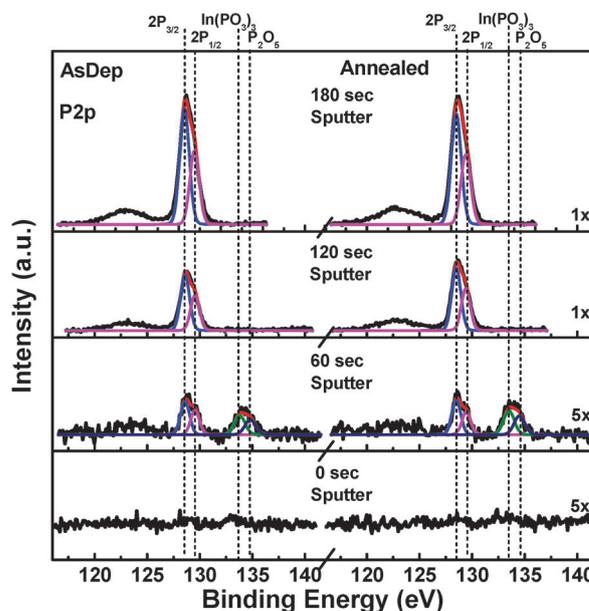


Fig. 4 XPS core level spectra of P 2p for as-deposited and annealed  $\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{InP}$  samples at different  $\text{Ar}^+$  sputtering times.

+6.1 eV relative to  $P_{2p_{3/2}}$  was assigned to  $P_2O_5$  and of +5.1 eV was assigned to  $In(PO_3)_3$ .<sup>35</sup> There was a possibility that a little amount of P-related oxide peak was found, due to re-oxidation during limited air exposure needed for sample handling or that may be the result of incomplete oxide removal or partial ALD self cleaning. Due to low resolution of the XPS spectra no clear observation of  $P_xS_y$  was retrieved which can be located in between 130 to 132 eV.<sup>36</sup> After sputtering for long time the substrate related peak becomes more pronounced as the electrons come from the InP surface after etching most of the  $Ta_{1-x}Zr_xO$  as evidenced after 120–180 s sputtering XPS spectra. Therefore having almost similar intensity for the oxide related peak of  $P_2O_5$  and  $In(PO_3)_3$  we assume that due to the thermodynamic stability of this gate stack no additional P-oxide growth occurred. A similar stability phenomenon was observed during  $In_{3d_{5/2}}$  XPS analysis for the  $Ta_{1-x}Zr_xO/InP$  interface.

Fig. 5 describes the  $P_{2p}$  spectra after ALD  $SiO_2$  passivation for the as-deposited and annealed sample. In contrast, the signal from the P-oxide for the  $SiO_2$  passivated sample after 0–120 s sputtering close to the detection limit of XPS before and after annealing, suggested that there was negligible P-diffusion taking place within the dielectrics after the  $SiO_2$  ALD interfacial layer. The weak signals for 0 and 60 s sputtering cases are due to electron effective attenuation which is more pronounced for the  $SiO_2$  passivated sample, because the attenuation length is shorter in the higher density  $SiO_2$  film. This may also be due to the higher overall thickness of the combined  $Ta_{1-x}Zr_xO/SiO_2$  stack. A P-oxide related peak has been fitted with similar binding energy separation as discussed earlier. Interestingly after 120–180 s sputtering the intensity of the P-oxide peak increased compared to without the passivated sample. The existence of these high intensity binding states was still a matter of doubt. The formation of  $SiPO_4$  also is a possibility, which would have a similar BE

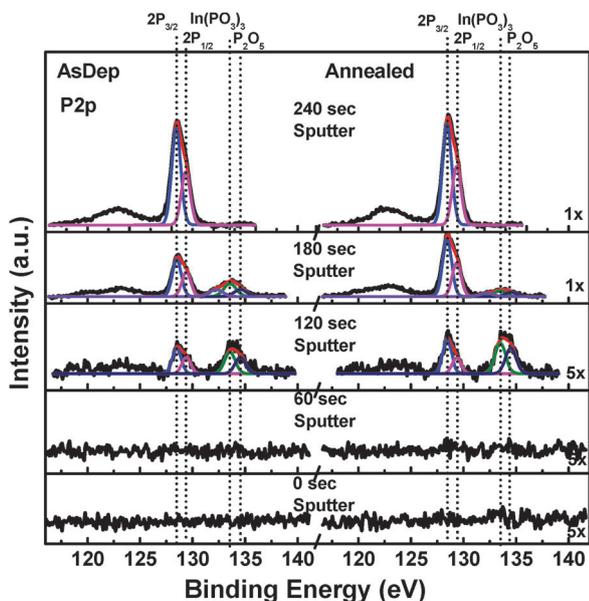


Fig. 5 XPS core level spectra of P 2p for as-deposited and annealed  $Ta_{1-x}Zr_xO/SiO_2/n-InP$  samples at different  $Ar^+$  sputtering times.

position to that of the peak assigned here to  $P_2O_5$ . A similar result has been reported by Adelman *et al.* who worked with  $Al_2O_3$  on InP which resulted to form  $AlPO_4$ .<sup>37</sup> However, the interfacial oxide after 180 s clearly becomes more phosphorous rich similar to In with an increase of the binding energy for P-oxide. However, after  $SiO_2$  passivation, the concentration of  $SiPO_4$  was detected to slightly increase after annealing which is likely due to the oxygen transfer from P to Si at the interface.

Fig. 6(a) presents the typical  $C-V$  characteristics of  $Ta_{1-x}Zr_xO/InP$  gate stacks at different frequencies. True accumulation was not obtained due to the saturation of the density of states in the low conduction band.<sup>38</sup> Also, the accumulation capacitance was lower at low applied AC frequencies compared to the oxide capacitance measured using quasi-static  $C-V$  (QSCV).  $Ta_{1-x}Zr_xO/InP$  gate stacks showed two distinct frequency dependent capacitance phenomena. Elevated inversion capacitance was observed and originated from the mid-gap energy trap density and uncontrolled dispersion in the accumulation region; these observations are similar to previous reports for high- $k/III-V$  systems.<sup>39</sup> The origin of this behavior is the presence of interface traps having an energy close to the InP conduction band.<sup>40</sup> Under inversion conditions, the effective inversion capacitance can be expressed as a series combination of  $Ta_{1-x}Zr_xO$ , IL capacitance and the capacitance in the hole inversion layer. The fixed charge,  $Q_f$ , induces a flatband voltage ( $V_{fb}$ ) shift in the gate electrode

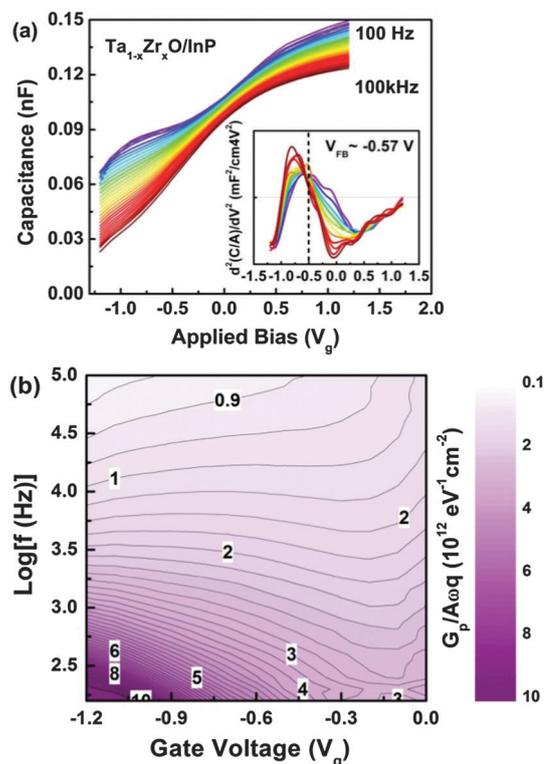


Fig. 6 (a) Measured room temperature multi-frequency capacitance as a function of applied gate voltage,  $V_g$ , for  $TaN/Ta_{1-x}Zr_xO/n-InP$  MOS capacitors and (inset) the second derivatives of the capacitance as a function of gate voltage. (b) Normalized parallel conductance map showing  $(G_p/A\omega q)$  as a function of gate voltage and frequency.

through capacitive coupling of the gate dielectric.  $V_{fb}$  was calculated from the method described by Winter *et al.*<sup>41</sup> According to their hypothesized relationship between accumulation and inversion, the point of intersection between the second derivative of the multi-frequency capacitance and the applied voltage,  $V_g$ , is independent of the measurement frequency. Using 100 Hz frequency extracted capacitance equivalent capacitance (CET =  $\epsilon_0 \times k_{SiO_2}/C_{ox}$ ) was found to be 1.8 nm. The equivalent dielectric constant ( $k_{SiO_2} \times T_{ox}/CET$ ) achieved through high calculations from CET was  $\sim 20$ .<sup>42</sup> Detailed calculations have been given in the ESI.† The inset in Fig. 6(a) shows the intersection of multi-frequency  $d^2(C/A)dV^2$  vs.  $V_g$  for the above gate stack.  $V_{fb}$  was found to be  $\sim 570$  mV for the Ta<sub>1-x</sub>Zr<sub>x</sub>O/InP stack. The large  $V_{fb}$  value for the Ta<sub>1-x</sub>Zr<sub>x</sub>O/InP gate is due to unwanted In diffusion during ALD deposition, as was evident from EDS and XPS analyses. The efficiency of the Fermi level response can be measured based on whether or not an applied  $V_g$  is sufficient to fully deplete the InP surface. Experimentally, this phenomenon is observed when the capacitance reaches a minimum given by the doping level of the semiconductor. As seen from the contour map in Fig. 6(b) for the Ta<sub>1-x</sub>Zr<sub>x</sub>O/InP MOS capacitor investigated here, the Fermi level movement is not quite sufficient to fully deplete the semiconductor; this behavior was caused by a high  $D_{it}$ . The conductance peaks signify energy loss from charging and discharging of the interface traps in response to the applied AC bias. Interface traps near the Fermi-level charge and discharge are because the small applied AC signal leads to changes in the interface trap occupancy and Fermi level oscillation at the interface.<sup>43</sup> To obtain a more quantitative measure of the midgap  $D_{it}$ , we plotted maps of the normalized parallel conductance,  $[(G_p/\omega)/Aq]$ , as a function of frequency and gate bias for the MOS capacitors with Ta<sub>1-x</sub>Zr<sub>x</sub>O gate dielectrics, Fig. 6(b). Here,  $G_p$  is the parallel conductance,  $\omega$  is the angular frequency,  $A$  is the MOS capacitor area and  $q$  is the elemental charge. The parallel normalized conductance is given by

$$\frac{\langle G_p \rangle}{A\omega q} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2(C_{ox} - C_m)} \quad (1)$$

where  $\omega$  is  $2\pi f$ ,  $f$  is the measurement frequency,  $C_{ox}$  is the gate oxide capacitance,  $G_m$  is the measured conductance and  $C_m$  is the measured capacitance.<sup>44</sup> The gate oxide capacitance was estimated from the QSCV measurement. Our  $G_p/A\omega q$  analysis in Fig. 6(b) confirmed the existence of Fermi level pinning because no clear peak was observed in the contour map. The absence of peaks (or a lack of peak shifting) indicated that the surface potential did not respond efficiently to the gate bias because the Fermi level was located between the conduction band edge and the mid-gap.

Fig. 7(a) and (b) show the effects of the SiO<sub>2</sub> interfacial layer on InP MOS capacitor performance. The Ta<sub>1-x</sub>Zr<sub>x</sub>O/SiO<sub>2</sub>/InP gate stack exhibited much smaller dispersion at accumulation than the Ta<sub>1-x</sub>Zr<sub>x</sub>O/InP gate stacks. Fig. 7(a) represents typical frequency dependent  $C$ - $V$  behaviors of the TaN/Ta<sub>1-x</sub>Zr<sub>x</sub>O/InP capacitors showing an increase in the  $C$ - $V$  hump with decreasing measurement frequency. Similar trends were observed for the parallel conductance peaks ( $G_p$ ), which were found at the

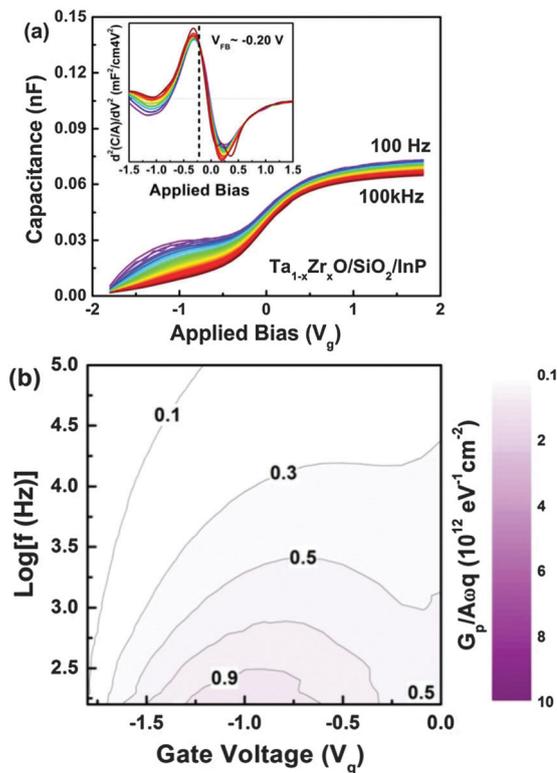


Fig. 7 (a) Multi-frequency capacitance–voltage characteristics as a function of applied gate voltage measured at room temperature for TaN/Ta<sub>1-x</sub>Zr<sub>x</sub>O/SiO<sub>2</sub>/InP MOS capacitors and (inset) the second derivative of the capacitance as a function of gate voltage. All the curves meet at the same point on the  $V_g$ -axis. (b) Normalized parallel conductance map, showing  $(G_p/A\omega q)$  as a function of gate voltage and frequency.

same voltages as the  $C$ - $V$  humps (not shown here).  $C$ - $V$  hump elimination was accompanied by a significant reduction  $D_{it}$ .<sup>45</sup> The smaller dispersion at accumulation was attributed to a smaller  $D_{it}$  in the Ta<sub>1-x</sub>Zr<sub>x</sub>O/SiO<sub>2</sub>/InP stack. Another criteria for accurate measurements of  $D_{it}$  can be obtained for high- $k$ /III-V interfaces provided that  $D_{it}$  is sufficiently low, for  $C_{ox} > qD_{it}$ , where  $C_{ox}$  is the accumulation capacitance density of the high- $k$  oxide and  $q$  the electronic charge.<sup>46</sup> The interface trap distribution in upper half of the InP band gap was extracted from the n-type TaN/Ta<sub>1-x</sub>Zr<sub>x</sub>O/SiO<sub>2</sub>/InP devices obtained from the conductance measurement and plotted in Fig. S2(a) in the ESI.† The  $D_{it}$  value near the conduction band at 0.27 eV was  $4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ . In case of the TaN/Ta<sub>1-x</sub>Zr<sub>x</sub>O/InP interface trap, density calculation results show that  $qD_{it} > C_{ox}$ . In this case the conductance method becomes not sensitive to extract  $D_{it}$  and the calculated values could be overestimated by an order of magnitude.<sup>47</sup> So for without the SiO<sub>2</sub> passivation sample it is difficult to calculate  $D_{it}$  effectively in a similar approach. A comparison of  $D_{it}$  characteristics with other published recent data have been described in the ESI† in Fig. S2(b). Our result shows that the extracted  $D_{it}$  values are comparable to recently published articles. The SiO<sub>2</sub> passivation layer reduced inversion capacitance because the passivation layer minimized In-related oxide growth. In addition, the inversion capacitance had another

capacitance component due to  $\text{SiO}_2(\text{C}_{\text{SiO}_2})$ . The minimum inversion capacitance value observed after  $\text{SiO}_2$  passivation at 1 MHz was close to the ideal capacitance, which indicates that the improvements in both Fermi level movement and surface potential resulted in full depletion of electrons at the InP semiconductor surface.<sup>44</sup> The dispersion at accumulation after introducing  $\text{SiO}_2$  was about 11.3% in the 100 Hz–100 kHz frequency range compared to 21.1% for without the  $\text{SiO}_2$  passivated sample. Low frequency dispersion for the  $\text{SiO}_2$  passivated sample indicates no significant change in the density of border traps located near the conduction band edge of InP.<sup>48</sup> The inset in Fig. 7(a) shows the second derivative of the  $C$ - $V$  characteristics after  $\text{SiO}_2$  passivation. Here, the  $\text{SiO}_2$  passivation resulted in a decrease in  $V_{\text{fb}}$ . This suggests that the  $\text{SiO}_2$  passivation counters In diffusion and reduces the number of positive fixed charges at the  $\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{InP}$  interface. A similar substrate diffusion effect on  $V_{\text{fb}}$  and its improvement after introducing a barrier layer was observed.<sup>49,50</sup> The lower normalized parallel conductance peak values for the  $\text{SiO}_2$  passivated MOS capacitor, Fig. 7(b) and its narrower trace, suggested a lower  $D_{\text{it}}$  and larger band bending occurred in response to a change in the applied gate bias.<sup>51</sup> The mechanisms that cause the reduction in mid-gap  $D_{\text{it}}$  are  $\text{SiO}_2$  passivation and a reduction in the native oxides at the interface of the III-V semiconductor. This phenomenon was in agreement with the HRTEM and XPS analyses discussed above.

Leakage current-electric field curves were measured for  $\text{TaN}/\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{InP}$  MOS capacitors with different  $\text{SiO}_2$  thicknesses by sweeping the electrical field from 0 to  $3.5 \text{ MV cm}^{-1}$  in the accumulation field region and recording the leakage current density under substrate electron injection (Fig. 8). To systematically monitor the effect of the  $\text{SiO}_2$  passivation layer, we compared the leakage current over 0, 5 and 10 ALD cycles. Although all these samples have different thicknesses, which may result in different leakage currents, the thickness does not influence our conclusion since we compared  $E_{\text{eff}}$  ( $E = V/d$ , where  $E$  is the electrical field,  $V$  is the applied voltage and  $d$  is the oxide thickness) instead of voltage. The leakage current densities at  $1 \text{ MV cm}^{-1}$  for  $\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{InP}$ ,  $\text{Ta}_{1-x}\text{Zr}_x\text{O}/5 \text{ cycle SiO}_2/\text{InP}$  and  $\text{Ta}_{1-x}\text{Zr}_x\text{O}/10 \text{ cycle SiO}_2/\text{InP}$  were  $3.2 \times 10^{-10} \text{ A}$ ,  $8.2 \times 10^{-12} \text{ A}$  and  $8.3 \times 10^{-13} \text{ A}$ , respectively. It is evident from Fig. 8 that the leakage current of the  $\text{SiO}_2$  passivated sample is much smaller than the sample without passivation. This suggests that a thin  $\text{SiO}_2$  layer significantly reduced the leakage because its bandgap is larger than that of the high- $k$  dielectric. For  $\text{TaN}/\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{InP}$  MOS capacitors, the leakage current is dominated by trap assisted Poole-Frenkel (P-F) tunneling. This is apparent in the abrupt increase in slope starting from a field of  $0 \text{ MV cm}^{-1}$ . Substrate diffusion was the main factor contributing to the generation of these traps in high- $k$  dielectrics. MOS capacitors with 5 and 10  $\text{SiO}_2$  ALD cycles showed two types of slopes in the accumulation region. Slopes in the leakage current above  $0.75 \text{ MV cm}^{-1}$  for the 5 cycle ALD case and above  $1.2 \text{ MV cm}^{-1}$  for the 10 cycle ALD case were significantly steeper than the slopes observed below these field strengths. Therefore, the regimes below  $0.75 \text{ MV cm}^{-1}$  for the 5 cycle case and below  $1.2 \text{ MV cm}^{-1}$  for the 10 cycle case were mainly dominated by trap-assisted tunneling

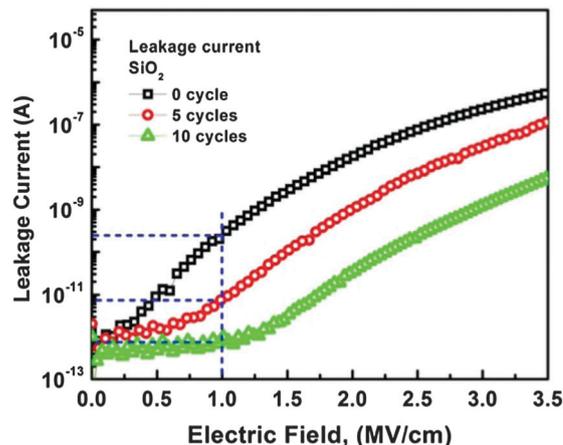


Fig. 8 Comparison of leakage current vs. electric field characteristics for  $\text{TaN}/\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{InP}$  MOS capacitors for various numbers of  $\text{SiO}_2$  (0, 5 and 10 cycles) cycles.

or P-F tunneling and the regimes above these field strengths were effectively dominated by Fowler-Nordheim (F-N) tunneling.<sup>52</sup> Similar recent findings on nanolaminated  $\text{Al}_x\text{Ti}_y\text{O}$  on the III-V substrate by Ui *et al.* show that upon increasing the barrier height Poole-Frenkel conduction changed to F-N tunneling for  $\text{Al}_2\text{O}_3$ .<sup>53</sup> Also Krylov *et al.* clearly observed using X-ray photo-emission spectroscopy and time of flight secondary ion mass spectrometry, the higher substrate diffusion process enhances the leakage current and reduces the break down voltage.<sup>21</sup> They have correlated their chemical and electrical analysis with the findings that leakage is enhanced by substrate out-diffusion. So these results support our assumption regarding leakage current reduction due to  $\text{SiO}_2$  passivation which blocks substrate diffusion. The 5 cycle ALD case showed F-N tunneling under a lower electrical field than in the 10 cycle ALD case; this is consistent with the thinner  $\text{SiO}_2$  layer in the 5 cycle ALD case. As the thickness of the  $\text{SiO}_2$  increased, the leakage current decreased, as shown in Fig. 8. As discussed earlier, silicate formation reduced the interface states near the Fermi level (above the InP valence band maximum). Because leakage current flows *via* interface states, the silicate formation also resulted in a decrease in leakage current.<sup>54</sup> Therefore, a thin silicate IL is important for suppressing the leakage current. Low leakage current density was also attributed to the high band gap of  $\text{SiO}_2$ , which formed a high band offset that reduced electrical conduction.

## Conclusion

In summary, an amorphous  $\text{Ta}_{1-x}\text{Zr}_x\text{O}$  dielectric film was successfully deposited on an InP substrate by thermal ALD with a Ta:Zr ratio of 3:2. The  $\text{Ta}_{1-x}\text{Zr}_x\text{O}$  film exhibited good insulating characteristics and thermal stability even after annealing at  $500 \text{ }^\circ\text{C}$ . Clear evidence for In diffusion to the surface after post-deposition annealing of  $\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{InP}$  stacks was provided by XPS and EDS. XPS analysis with  $\text{In}3d_{5/2}$  and  $\text{P}2p$  spectra revealed that a silicate layer existed at the interface between Si and In/P after  $\text{SiO}_2$  passivation using ALD. Electrical measurements,

including  $C$ - $V$  at different frequencies, parallel conductance method measurements and  $I$ - $V$  measurements were conducted. CET of  $\sim 1.8$  nm along with a high dielectric constant was found to be 20. The results demonstrated that the high density of interface traps can be passivated by thin  $\text{SiO}_2$  ALD deposition. TEM images showed that the thickness of the interfacial layer decreased upon  $\text{SiO}_2$  passivation, confirming the negligible out-diffusion of metallic In and suggesting oxygen depletion as well. The overall reduction in the interfacial layer and improvement in the electrical results is further supported by the Fermi level movement observed in the parallel conductance contour plot. Overall, capacitance and parallel conductance results obtained during electrical characterization suggest that  $\text{SiO}_2$  improves the quality of the  $\text{Ta}_{1-x}\text{Zr}_x\text{O}/\text{InP}$  interface. Even though the effective dielectric constant decreases after  $\text{SiO}_2$  passivation, this trade-off between improvement in electrical results and reduction in dielectric constant is acceptable.  $I$ - $V$  measurements correlated with the XPS results led us to conclude that P-F and F-N tunneling is the dominant current transport mechanism in the samples studied.

## Experimental section

For this study, a commercial ALD chamber (ALD5008 of SNTek Co.) was used. This setup has a double showerhead system for improving the film uniformity.  $\text{H}_2\text{Si}[\text{N}(\text{C}_2\text{H}_5)_2]_2$  (SAM24) was used as a precursor for  $\text{SiO}_2$ ,  $(\text{C}_5\text{H}_5)\text{Zr}[\text{N}(\text{CH}_3)_2]_3$  (ZyALD) was used for  $\text{ZrO}_2$  and  $\text{Ta}(\text{OC}_2\text{H}_5)_5$  was used for  $\text{Ta}_2\text{O}_5$ . To obtain sufficient vapor pressure, these precursors were evaporated in stainless-steel bubblers at  $40^\circ\text{C}$ ,  $40^\circ\text{C}$  and  $160^\circ\text{C}$ , respectively. Ar gas was controlled using a mass flow controller (MFC) and was introduced into the reaction chamber to purge the excess gas molecules, remove the reaction by products and control the exposure steps.  $\text{O}_3$  gas was used as an oxidant for ALD and the  $\text{O}_3$  concentration was fixed at 18% using the MFC. An ALD super-cycle process was carried out for Zr doping in  $\text{Ta}_2\text{O}_5$ . Specifically, one ALD  $\text{ZrO}_2$  cycle was followed by several repeated ALD  $\text{Ta}_2\text{O}_5$  cycles ( $\text{ZrO}_2:\text{Ta}_2\text{O}_5$ : 1 : 8). This super-cycle process allowed us to easily manipulate the  $\text{Zr}/(\text{Zr} + \text{Ta})$  composition of the ALD Zr doped- $\text{Ta}_2\text{O}_5$  films. During this process, the substrate temperature was maintained at  $250^\circ\text{C}$ .

III-V MOS capacitors were fabricated on  $n$ -InP ( $3\text{--}5 \times 10^{17} \text{ cm}^{-3}$ ) with (100) orientation doped with Si using the following procedures. For an InP substrate native oxide removal and S-passivation was done by dipping in water-based 1% hydrofluoric acid and 21%  $(\text{NH}_4)_2\text{S}$  solutions for 1 min and 5 min, respectively, to minimize the surface oxidation. The substrate was then rapidly moved to the ALD chamber.  $\text{SiO}_2$  films were deposited by ALD for 5 and 10 cycles prior to the deposition of Zr doped  $\text{Ta}_2\text{O}_5$ . A single Zr doped  $\text{Ta}_2\text{O}_5$  MOS capacitor was fabricated for comparison using the same process without ALD deposition of  $\text{SiO}_2$ . After oxide deposition, post deposition annealing (PDA) was performed using a rapid thermal annealing (RTA) system in a  $\text{N}_2$  ambient at  $500^\circ\text{C}$  for 20 s. To form a gate electrode, a TaN top electrode was deposited using a lift-off

process and was then annealed in forming gas. To create the back contact of the capacitors, the samples were connected to a Cu tape on glass using silver paste.

The thicknesses and refractive indexes of the films were measured using spectroscopic ellipsometry. The chemical composition and impurity levels were analyzed by X-ray photoelectron spectroscopy (XPS) using a monochromatic Al  $K\alpha$  source (beam energy of 1486.6 eV and analysis area of  $100 \mu\text{m}^2$ ). The surface C 1s peak at 284.5 eV was used as a reference to calibrate the measured core levels. Data were fitted with individual peaks using XPSPEAK software with a mixed Gaussian and Lorentzian peak function and a Shirley type background. Because the gate stack thickness was greater than the XPS detection limit, the high- $k/\text{InP}$  interface could not be observed using a single XPS run. Therefore, we used Ar sputtering followed by XPS measurements to measure the composition change as a function of depth. The electrical properties, including capacitance-voltage ( $C$ - $V$ ) and current-voltage ( $I$ - $V$ ) characteristics were evaluated by using an Agilent LCR meter, a Keithley voltage source.

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