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Atomic layer deposited Al_2O_3 on high quality *p*-type epitaxial-GaAs/Ge for advanced III–V/Ge based device application

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ABSTRACT

Development of high quality *p*-type epitaxial gallium–arsenide (epi-GaAs) on germanium (Ge) with sub-nm surface roughness is much sought after for the next generation high speed transistors application. High quality zinc doped *p*-type epitaxial GaAs with surface roughness of ~0.87 nm was grown on Ge substrates at 675 °C. Thin $Al_{0.3}Ga_{0.7}As$ buffer layer and un-doped GaAs of 300 nm thick were introduced to suppress the Ge defects and auto-doping into epi-GaAs layer. The material and optical properties of the *p*-type epi-GaAs/un-doped GaAs/$Al_{0.3}Ga_{0.7}As$/Ge structures were examined through PL and Raman analysis. The metal–oxide–semiconductor capacitor (MOSC) was fabricated using *p*-type epi-GaAs layer and atomic-layer-deposited Al_2O_3 gate dielectric. The effective dielectric constant of the Au/Al_2O_3/*p*-epi-GaAs gate-stack is 5.9 and hysteresis voltage of 500 mV was observed. The epi-GaAs layer is *p*-type in nature with doping densities of 5×10^{17} cm^{-3}.

1. Introduction

Epitaxial GaAs (epi-GaAs) on Ge substrate has received much attention to realize high performance, flexibility, and enhanced functionality of GaAs compounds coupled with the low manufacturing cost and sheer scale of the silicon process technology [1–3]. For an example, high speed complementary metal–oxide–semiconductor (CMOS) device can be realized by integration of GaAs and Ge on a silicon platform [4–12]. On the other hand, optical devices such as long-wavelength InAs/GaAs quantum-dot laser diode on Ge substrate were also demonstrated by Liu et al. [13]. It is worth to note that the performance gains using an epitaxial layer is still challenging due to the several reasons. Epitaxial-GaAs suffers from poor surface quality. Ge out-diffusion and auto-*n*-type doping in the epi-GaAs is also critical for the device application [5–8]. GaAs has six times higher electron mobility than Si, suitable for *n*-type metal–oxide–semiconductor field-effect-transistor (nMOSFET) applications. However, Ge has four times higher hole mobility compared with Si, suitable for *p*-type MOSFET applications. Thus, development of *p*-type epitaxial GaAs is crucial to achieve *n*-MOSFET device using epi-GaAs layer as a channel layer. Toward this, we have developed *p-type* epitaxial GaAs on Ge substrate by suppressing Ge out-diffusion through integrating AlGaAs buffer layer and un-doped GaAs layer. We have demonstrated *p*-type epi-GaAs metal–oxide semiconductor capacitors (*p*-type epi-MOSC) on Ge substrate using ALD Al_2O_3 gate dielectric on epi-GaAs layer.

There are several challenges related to integration of GaAs/Ge on a silicon platform such as formation of anti-phase domain (APD) defects, Ge out-diffusion and auto-doping, and high surface roughness. By using Ge substrate 6° offcut toward (111) direction, APD defects can be eliminated [2,6]. On the other hand, inter-diffusion of atoms can be suppressed significantly by introducing AlAs [6]. The high quality epi-GaAs with sub-nm surface roughness was also achieved through the introduction of $Al_{0.3}Ga_{0.7}As$ buffer layer. The epi-GaAs layer is intrinsically *n*-type due to the Ge auto-doping [2,7,8]. Thus, for the development of *p*-type epi-GaAs, zinc dopant should be higher than the intrinsic doping concentration [14]. Furthermore, interface quality at the *p*-type epi-GaAs layer and dielectric is a critical towards the development of *p*-type epi-GaAs based devices [2,8]. It plays a key role for surface channel

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MOSFET devices. Presence of GaAs-oxide (native oxide) degraded device performance. Formation of native oxide is prone to epi-GaAs compared with bulk-GaAs, as epi-GaAs has high surface roughness [8]. The ALD Al_2O_3 shows promising results with bulk-GaAs substrates. ALD Al_2O_3 also reduces native As-oxides through a "self-cleaning". Moreover, ALD is very crucial for epi-GaAs systems compared to the other deposition technique, since it provides better interface between epi-GaAs and dielectric through conformal coating of the epi-GaAs layers. In the present work, we have developed *p*-type epitaxial GaAs with sub-nm surface roughness by using AlGaAs buffer layer and undoped GaAs layer for the high speed logic and memory application. ALD Al_2O_3 dielectric has been integrated to study the epi-GaAs layer and interface quality between epi-GaAs and dielectric layer.

2. Experiment

P-type epi-GaAs was deposited using MOCVD technique at 675 °C on *p*-type Ge (100) substrates with 6° offcut toward the (111) plane to eliminate the APD defects. The doping concentration of Ge substrate was $\sim 10^{16}$ cm^{-3}. The Ge substrate was first heated up to 720 °C in H_2 ambient and kept at that temperature for 5 mins to remove the native oxide layer in the absence of As. Then, the temperature is ramped down to 675 °C, and AsH_3, TMGa, and TMAl are introduced into the reactor for the growth of 10-nm thin $Al_{0.3}Ga_{0.7}As$ buffer layer and 300 nm thick un-doped GaAs layers at a growth rate of 0.42 nm/s. Thin $Al_{0.3}Ga_{0.7}As$ buffer layer and un-doped GaAs were introduced to suppress the Ge out-diffusion and intrinsic Ge auto-doping into epi-GaAs layer. Zinc (Zn) doped *p*-type epi-GaAs of 200 nm thick was grown on un-doped GaAs layer using MOCVD technique at 675 °C. The doping concentration of Zn was 10^{18} cm^{-3}. For epi-GaAs metal–oxide–semiconductor (epi-GaAs MOS) device fabrication, the wafers were degreased using isopropanol, cleaned in 1% hydrofluoric acid solution for 3 mins to remove native oxide. After cleaning, sample was loaded into an atomic layer deposition (ALD) chamber for Al_2O_3 deposition. Thin film Al_2O_3 of thickness ~12 nm was deposited at 250 °C using TMA and H_2O precursors. Post deposition annealing (PDA) was carried out in N_2 ambient at 500 °C for 1 min by rapid thermal annealing (RTA). Electrical measurements were performed on GaAs MOS capacitor structure. The Au metal, deposited by sputter, was used as the gate electrode (area: 1.9×10^{-3} cm^2). Low resistance Ohmic contact was made by using Ti/Pt/Au on the back side of *p*-Ge wafers through sputter.

3. Results and discussion

Surface roughness plays a critical role for GaAs/Ge based devices. Thus, it is essential to grow the high quality epitaxial-GaAs with sub-nm surface roughness. Surface morphology of epi-GaAs without ALD coated Al_2O_3 was performed by using atomic force microscopy (AFM), as shown in Fig. 1. Surface roughness of zinc doped epi-GaAs was found to be ~0.87 nm. The surface roughness of *p*-type epi-GaAs layer is much lower to the reported results [14]. Indeed, to the best of our knowledge; this is the lowest reported value for the *p*-type epi-GaAs layer. The Al_2O_3 coated epi-GaAs also shows similar surface topography. Phonon Raman scattering and photoluminescence can provide a measurement of the stress and presence of defects in a material. Fig. 2 (a) shows room temperature Raman scattering spectra of epi-GaAs layer grown on a Ge substrate with thin AlGaAs buffer layer. The Raman spectrum of epitaxial GaAs epilayer shows both transverse optical (TO) phonon at ~268 cm^{-1} and a longitudinal optical (LO) phonon at ~293 cm^{-1}, similar to the reported results [15,16]. In

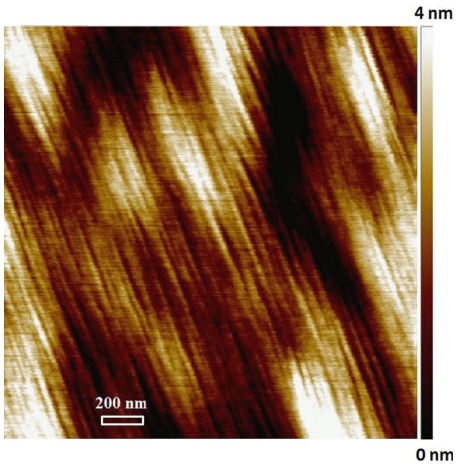

Fig. 1. AFM image of *p*-type epitaxial GaAs grown on Ge substrate.

case of GaAs, the LO mode is Raman-active while the TO mode is thought to be caused by structural disorder, surface roughness, alloy disorder and impurities [17]. The LO peak of the epi-GaAs layer grown at 675 °C was sharp indicating crystalline behavior. In addition to a strong LO phonon band in epi-GaAs, a weak TO band was also appeared. The PL spectrum of epi-GaAs measured at room temperature and is presented in Fig. 2(b). Single emission peak suggests that there is no significant Ge diffusion into the epi-GaAs layer. The main peak at room temperature corresponds to an energy value of 1.410 eV representing GaAs near-band-edge emission. Emission from 1.2 eV to 1.3 eV which is related to Ge diffusion into GaAs was found negligible [6].

Suppression of elemental Ge out-diffusion was observed in the secondary ion mass spectrometry (SIMS) profile, as shown in Fig. 3(a). The elemental Ge atoms out-diffuse up to ~25 nm into the undoped-GaAs layer, which agrees well with reported results [2]. It is worth to note that even though AlGaAs effectively reduced the Ge atom diffusion into GaAs, there is still Ge atoms. The concentration of Ge is below SIMS detection limit (approximately 10^{15} cm^{-3}) [2,14]. To reduce the background doping concentration due to the Ge auto-diffusion, we have introduced 300 nm undoped GaAs layer between *p*-type epi-GaAs layer and Ge substrate. Fig. 3(b) depicts the cross-section HRTEM of epi-GaAs on 6° off-cut Ge(100) substrates. The thickness of zinc doped epi-GaAs layer and undoped epi-GaAs is 200 nm and 300 nm, respectively. HRTEM shows a smooth and abrupt interface between epi-GaAs and the Ge substrate. Further, it confirms that the epi-GaAs layers are free from any APD defects. To fabricate the metal–oxide–semiconductor devices with *p*-type epitaxial GaAs layer, Al_2O_3 of thickness 12 nm was deposited on *p*-type epi-GaAs using ALD. It is worth noting that there was no indication of forming interfacial layer between *p*-type epi-GaAs and Al_2O_3, as shown in HRTEM image. This is due to the self-cleaning property of ALD Al_2O_3. A 20-cycle in-situ trimethylaluminium cleaning was performed to remove native oxide and excess As from the epi-GaAs layer prior to the Al_2O_3 deposition, resulting almost no interfacial layer between Al_2O_3 and epi-GaAs layer. The Al_2O_3 layer is partially crystallized. As it has been reported that the amorphous phase of Al_2O_3 is expected to be thermodynamically stable but if a critical thickness of Al_2O_3 is reached, a poly crystalline may be preferred. Above the critical thickness amorphous alumina phase becomes unstable and a crystal phase is preferred [18].

Capacitance–voltage (*C*–*V*) and current–voltage (*I*–*V*) characteristics of Al_2O_3/epi-GaAs MOS device are shown in Fig. 4. The inset of Fig. 4 shows the schematic diagram of epi-GaAs MOS capacitors with ALD Al_2O_3 gate dielectric. Fig. 4(a) shows *C*–*V* characteristics of epi-GaAs MOS capacitors. *C*–*V* characteristics showed evidence of hole accumulation for negative biases and electron inversion for

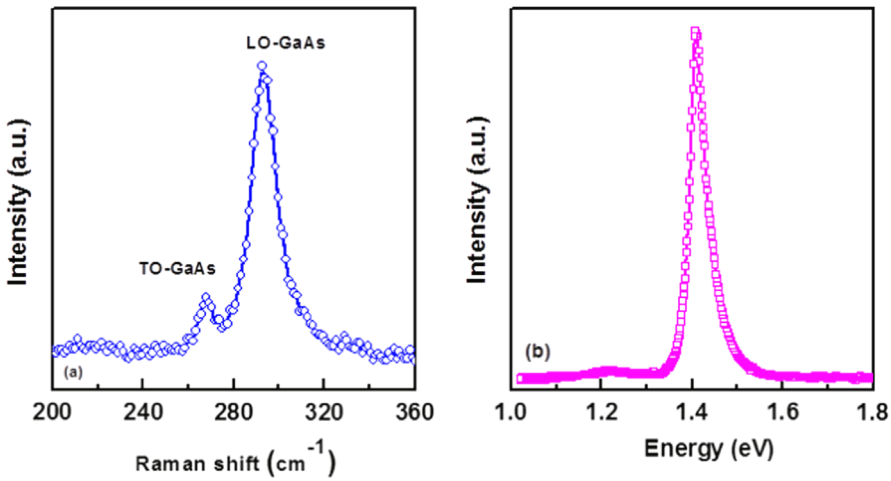

Fig. 2. (a) Raman scattering spectra of epi-GaAs grown by MOCVD technique at 675 °C. (b) PL spectra of epi-GaAs/$Al_{0.3}Ga_{0.7}As$/Ge structures measured at room temperature.

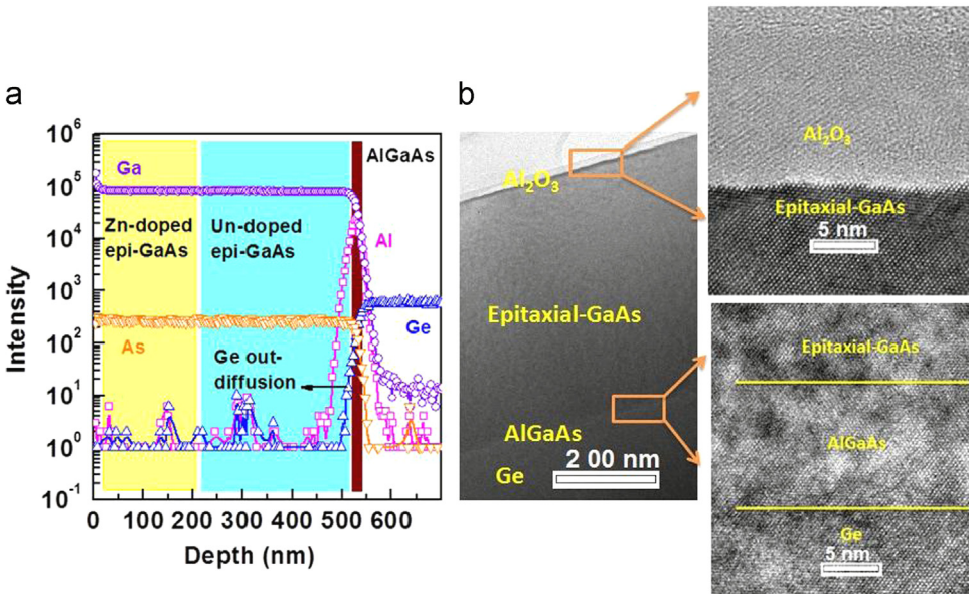

Fig. 3. (a) SIMS profiles for *p*-type epi-GaAs layer with $Al_{0.3}Ga_{0.7}As$ buffer layer and undoped GaAs layer and (b) cross-sectional HRTEM images of epi-GaAs/$Al_{0.3}Ga_{0.7}As$/Ge with Al_2O_3 films of 12 nm.

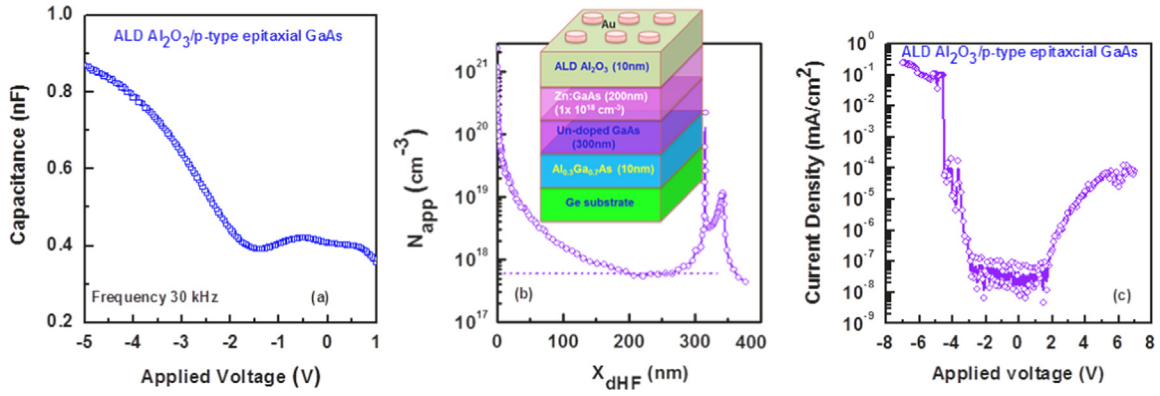

Fig. 4. (a) Capacitance–voltage characteristics of Al_2O_3/epi-GaAs at the applied frequency of 30 kHz, (b) apparent doping profiles for the epi-GaAs obtained from *C*–*V* characteristics and (c) current–voltage characteristics of Al_2O_3/*p*-type epi-GaAs gate stack. The inset (b) shows the schematic diagram of *p*-type epi-GaAs MOSC.

positive biases, which suggests the *p*-type epi-GaAs MOSC behavior. Interface trap density (D_{it}) was calculated from conductance technique. The minimum D_{it} found for *p*-type epi-GaAs MOSC was $\sim 8 \times 10^{12}\ eV^{-1}cm^{-2}$. The interface trap density is comparable with the reported results of high-k/bulk GaAs gate stack [19–26]. From the high frequency *C*–*V* characteristics, the depletion depth

(X_{dHF}) and apparent doping (N_{appHF}) were extracted [27]. Fig. 4 (b) shows the apparent doping profile of the epi-GaAs layer. The apparent doping concentration of the epi-GaAs layer is $\sim 5 \times 10^{17}$ cm^{-3}. Leakage current characteristics have been performed for further investigation of the *p*-type epi-GaAs MOSC. Fig. 4(c) shows the *I*–*V* characteristics of the Al_2O_3/*p*-epi-GaAs MOSC. Asymmetrical characteristics of *I*–*V* curves under forward and reverse biases were observed. An average breakdown field of ~3.3 MV/cm is observed for Al_2O_3/*p*-epi-GaAs gate stack. It is worth noting that the interface quality needs to improve further for device application. The interface quality and gate dielectric properties can be improved by using bi-layer dielectric, alloy dielectric, and interfacial passivation layer [7,20,22,28–32]. Recently, we have shown by employing vacuum based annealing, the dielectric quality as well as interface quality can be improved significantly [29].

4. Conclusion

We have successfully grown zinc doped epi-GaAs with surface roughness around 0.87 nm. There is no significant structural defect after introduced zinc dopant in the epi-GaAs layer. The capacitance–voltage characteristic shows zinc doped epi-GaAs is *p*-type in nature. Hysteresis voltage and leakage current are comparable with high-k/bulk-GaAs gate structure. The feasibility study of *p*-type epi-GaAs with ALD Al_2O_3 will help to design the *p*-type epi-GaAs based MOSFET on a silicon platform for high speed logic and memory applications.

Synopsis

High quality zinc doped *p*-type epitaxial GaAs with surface roughness of ~0.87 nm was grown on Ge substrates at 675 °C. Thin $Al_{0.3}Ga_{0.7}As$ buffer layer and un-doped GaAs of 300 nm thick were introduced to suppress the Ge-auto-doping and Ge-based complex defects into epi-GaAs layer. The metal–oxide–semiconductor capacitor (MOSC) was fabricated using *p*-type epi-GaAs layer and atomic-layer-deposited Al_2O_3 gate dielectric. The epi-GaAs layer is *p*-type in nature with doping densities of 5×10^{17} cm^{-3}.

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