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Electrical properties of the HfO_2–Al_2O_3 nanolaminates with homogeneous and graded compositions on InP

Chandreswar Mahata [a], Youngseo An [b], Sungho Choi [b], Young-Chul Byun [c], Dae-Kyoung Kim [d], Taeyoon Lee [a], Jiyoung Kim [c], Mann-Ho Cho [d], Hyoungsub Kim [b, *]

[a] School of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, Republic of Korea
[b] School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon 16419, Republic of Korea
[c] Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, TX 75080, USA
[d] Institute of Physics and Applied Physics, Yonsei University, Seoul 03722, Republic of Korea

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ABSTRACT

For possible application to a gate dielectric in high-performance III-V transistors, nanolaminated HfO_2–Al_2O_3 films with artificial compositional profiles were deposited on n-type InP substrates using atomic layer deposition. The films were vertically graded (HfO_2 and Al_2O_3 at the surface and interface regions, respectively) and had a homogeneous composition. To compare their electrical properties, a similar physical thickness and capacitance-equivalent thickness (CET) were maintained, and the graded structure showed an increase in the Al_2O_3 content near the high-*k* and InP interface region without an increase in CET, which suppresses the In incorporation at the near-interface region and reduces the density of the interface trap. However, doing so results in a degradation of the leakage current characteristics under voltage stressing when compared to homogeneously-nanolaminated films.

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1. Introduction

A primary pathway to further improve the performance of metal-oxide-semiconductor field-effect transistors (MOSFETs) in high-performance logic devices involves innovation in new materials rather than in simple feature-size scaling. In this respect, novel materials with a high-dielectric constant (high-*k*) can be integrated with III-V compound semiconductors to enable fast electron transport in order to continue the adherence to Moore's law for next-generation MOSFETs beyond the 5 nm feature-node [1–3]. However, one of the most difficult obstacles to realize III-V channel MOSFETs is to decrease the large density of electrical defects that exist near the high-*k* gate dielectric/III-V semiconductor interface [4,5].

For over a decade, a considerable amount of effort has been made to minimize the build-up of the near-interface defects by introducing various types of interfacial passivation layers (IPL) and surface passivation techniques [6–8]. Meanwhile, the engineering of high-*k* gate dielectric materials is another important area of focus to improve the quality of the interface while effectively maintaining a high *k* value. Although Al_2O_3 has a lower *k* value than HfO_2, experimental [9] and theoretical [10] studies have shown that it has a better interface quality with a III-V surface. As a consequence, the HfO_2 gate dielectric layer with an Al_2O_3-enriched interface region in stacked and/or uniformly nanolaminated forms has been extensively investigated by using several III-V substrates [11–14]. This compositional engineering of a high-*k* gate dielectric in the depth direction has been facilitated with the use of atomic layer deposition (ALD), which is a state-of-the-art, layer-by-layer deposition technique. Furthermore, the ALD method has an additional benefit in that it provides *in situ* self-cleaning of the surface oxide remnants on III-V substrates [15] in addition to producing a gate dielectric with excellent electrical properties. Nevertheless, an increase in the Al_2O_3 content for both the gate dielectric form in order to improve the interface quality results in a compromise resulting from the simultaneous decrease in the effective *k* value of the total gate dielectric layer.

Recently, buried-channel InGaAs MOSFET with an InP capping layer has been shown to exhibit improved performance relative to that of a surface channel device [16–18]. However, the most recent results that have been obtained show that the HfO_2 film on InP

* Corresponding author.
E-mail address: hsubkim@skku.edu (H. Kim).

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generates a large frequency dispersion in the accumulation than that on InGaAs [19]. Therefore, in order to realize high-performance buried-channel InGaAs MOSFETs, an improvement in the interface between HfO_2 and the InP capping layer should be accompanied. In this study, we have synthesized two HfO_2–Al_2O_3 nanolaminated films with a similar physical thickness and capacitance-equivalent thickness (CET) using an *in situ* ALD process on n-type InP substrates in order to better understand the effects of compositional engineering. One has been engineered with a graded compositional profile in the depth direction from the surface HfO_2 to the interface Al_2O_3, and the other maintained a continuous HfO_2-to-Al_2O_3 composition ratio. We then investigated and compared the effect that the two different composition profiles had on the final electrical properties of the MOS capacitors.

2. Experiments

MOS capacitors with different gate dielectrics (HfO_2–Al_2O_3 nanolaminates with different compositional profiles) were fabricated on unintentionally n-doped InP substrates (~5×10^{15} cm^{-3}). First, the native oxide was completely removed using a 1% HF solution, and the InP substrates were then passivated with sulphur by dipping in a 21% $(NH_4)_2S$ solution for 10 min and were immediately loaded into the ALD chamber. Tetrakis(ethylmethylamino)hafnium and trimethylaluminum precursors were then used to form the constituting ALD-HfO_2 and Al_2O_3 atomic layers, respectively, along with a common H_2O oxidant at 250 °C. Both the number and the sequence of each ALD-HfO_2 and Al_2O_3 forming step were varied to engineer two different types of nanolaminated structures *in situ*, as schematically depicted in Fig. 1. The S1 sample was engineered to have a compositional profile that varied from pure Al_2O_3 (interface region) to pure HfO_2 (surface region) in a stepwise manner. The S2 sample was homogeneously nanolaminated with a fixed concentration of Al_2O_3 for reference in order to produce a similar effective capacitance as that for the S1 sample. Detailed ALD schedules were then planned according to the deposition rates of ALD-HfO_2 and Al_2O_3 at 250 °C to produce a similar total physical thickness. After the gate dielectric had been formed, the samples underwent post-deposition annealing (PDA) at 500 °C for 60 s in an N_2 ambient. For the gate electrode, an Al-capped TaN film was sputter-deposited and patterned with an area of 7.85×10^{-5} cm^2 by using a lift-off process, followed by post-metallization annealing at 400 °C for 30 min in 4% H_2/N_2 mixed gas.

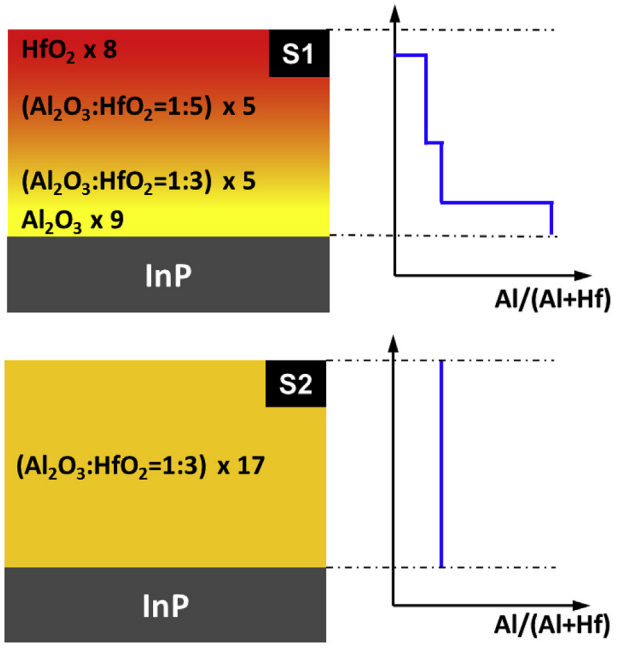

Fig. 1. Schematic diagrams of two nanolaminated HfO_2–Al_2O_3 dielectrics (S1 and S2 samples) on the InP used in this experiment, which include a number of ALD cycles for each deposition step. The figures on the right show the expected vertical composition profiles that were roughly calculated according to the HfO_2 and Al_2O_3 deposition rates.

The MOS capacitors that were fabricated were electrically characterized using an Agilent E4980A precision LCR metre and an Agilent B1500A semiconductor device analyser. The physical thickness and microstructure of the nanolaminated dielectrics in the samples were examined by using high-resolution transmission electron microscopy (HRTEM, JEOL JEM 2100F), and the overall composition and compositional depth profiles were measured with a medium energy ion spectroscope (MEIS, K-MAC MEIS-K120) with an He^+ beam with an incident energy of 100 keV in a double alignment mode in order to minimize the contribution from a crystalline InP substrate. These were also confirmed using additional time-of-flight secondary ion mass spectroscopy (ToF-SIMS, ION-TOF TOF.SIMS 5) in a depth profiling mode, where In and P were detected using a Bi^+ analysis gun after sputtering with O_2^+ and Cs^+ guns, respectively.

3. Results and discussion

The microstructure and the physical thickness of the different nanolaminated high-*k* dielectric materials were analysed *via* TEM, as shown in Fig. 2. The nearly-continuous change in the composition across the ultra-thin dielectric film resulted in no distinctive boundary (interface) in the S1 sample, and both samples exhibited amorphous layers due to the mixture of polycrystalline HfO_2 and amorphous Al_2O_3 atomic layers at a sub-nm scale. The thickness measured *via* TEM for the high-*k* films was quite similar as that of each other (5.3–5.5 nm). A MEIS measurement was conducted on two different nanolaminates for the compositional analysis, and the compositional depth profiles that were extracted are shown in Fig. 3. The results of the MEIS fitting indicate that the average composition of the entire nanolaminated films consisted of Hf:Al ratios of around 2.22 and 2.66 for the S1 and S2 samples, respectively. Both depth profiles obtained from the MEIS measurement are consistent with the intended compositional variations for Hf and Al, as shown in Fig. 1, and this proves that the compositional engineering was successful by manipulating the ALD schedule.

ToF-SIMS measurements were also performed in order to acquire the compositional depth profiles of In and P in greater detail, as shown in Fig. 4. Several studies investigating high-*k* films on InGaAs and InP substrates have shown that In diffusion takes place through defects in the high-*k* layer during PDA or even ALD [13,14,20,21]. In addition, the amount of In diffusion is largely dependent on the high-*k* identity, presumably due to the difference in the self-cleaning power of the metal organic precursors [13,20,21]. The In-rich interface and its diffusion into the high-*k* film may negatively impact the electrical properties of the final material that are closely associated with near-interface defects [13,22]. According to our previous study [13,14], In out-diffusion can be effectively suppressed by introducing more Al_2O_3 into homogeneously nanolaminated HfO_2–Al_2O_3 films on InP or inserting an ultra-thin Al_2O_3 layer in a stacked structure on InGaAs. As a result, a higher Al_2O_3 concentration close to the interface region between the high-*k* and InP layer can be predicted to result in less In incorporation at the near-interface region. The compositional variation of the ALD HfO_2–Al_2O_3 nanolamination processes shown in Fig. 1 suggests that a more Al_2O_3-rich interface will form in the case of S1 when compared to that for S2, and this is exactly

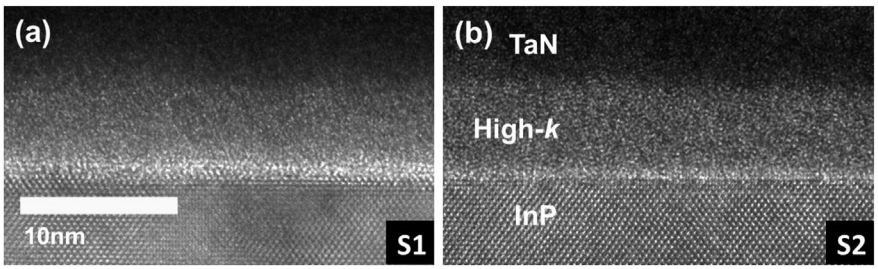

Fig. 2. Cross-sectional HRTEM images of the (a) S1 and (b) S2 samples after PDA at 500 °C for 60 s in N_2. The images were taken from the capacitor samples with a TaN electrode.

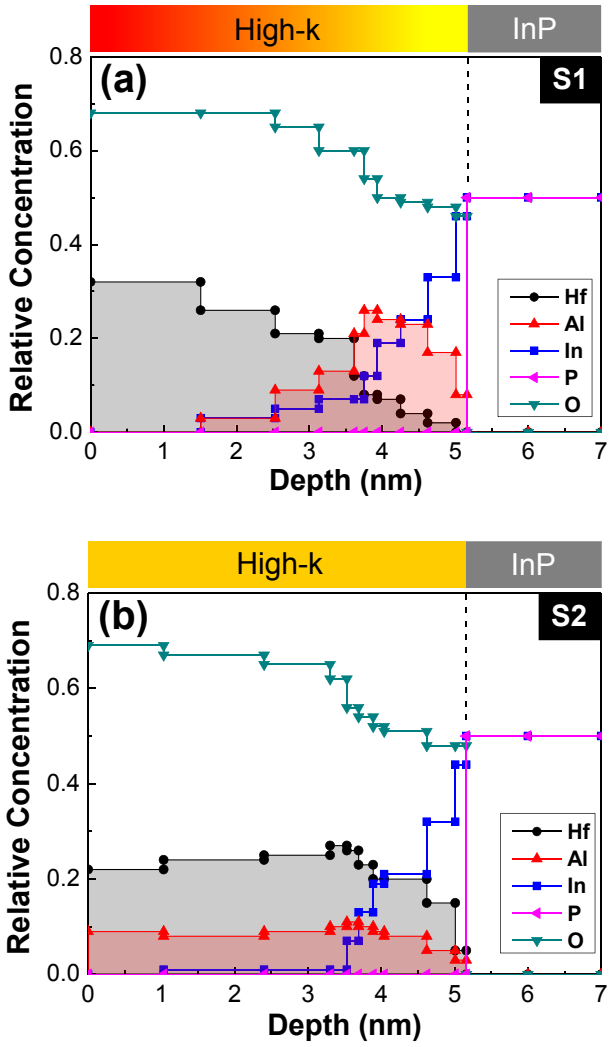

Fig. 3. Compositional depth profiles of the (a) S1 and (b) S2 samples based on the results of the simulation of the MEIS measurement. The samples underwent PDA at 500 °C for 60 s in N_2.

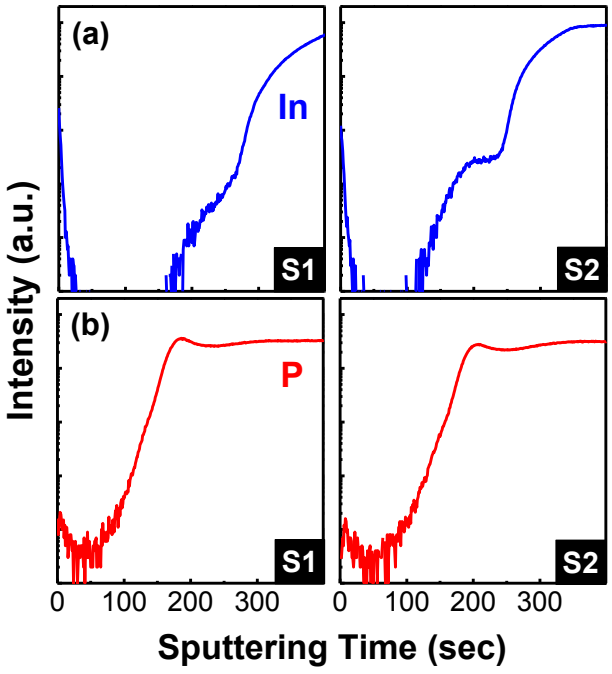

Fig. 4. ToF-SIMS depth profiles (a) In and (b) P atoms, taken from the S1 and S2 samples after PDA at 500 °C for 60 s in N_2.

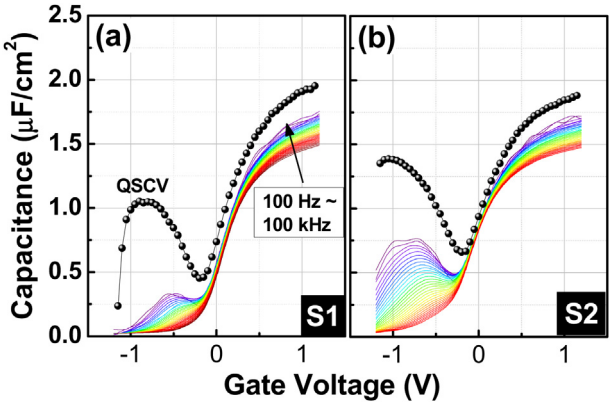

Fig. 5. Frequency-dependent *C*–*V* curves of the (a) S1 and (b) S2 samples measured from 100 Hz to 100 kHz in a logarithmic step. The symbols represent quasi-static *C*–*V* curves measured in the same voltage scale.

reflected by the In profiles observed in Fig. 4(a). Thus, enriching the interface region with more Al_2O_3 is more favourable in order to minimize the In incorporation at the near-interface region, which may exacerbate the interfacial properties of the HfO_2-Al_2O_3 nano-laminated film. In the case of the P distribution (see Fig. 4(b)), no distinguishable difference was detected among the samples.

Fig. 5 shows the capacitance–voltage (*C*–*V*) characteristics as a function of the AC frequencies applied in a single direction from inversion to accumulation. For all samples, the amount of frequency dispersion in the accumulation region, which is closely associated with high frequency-responding traps located near/at the interface region [9,23], is nearly 5–6% per decade within a frequency range from 100 Hz to 100 kHz. Quasi-static *C*–*V* (QSCV) curves were also

measured to obtain more accurate CET values from the nanolaminated samples, and these are included in Fig. 5. The CET values that were calculated after reading the capacitance with a gate voltage of 1.2 V were ~1.8 nm, which is close to each other. Since the physical thicknesses measured for all samples were similar with each other (see TEM images shown in Fig. 2), a similar CET implies a similar effective dielectric constant for the entire dielectric film. The S1 sample showed a slightly lower average Hf:Al atomic ratio than the S2 sample, but the CET value was similar. Although the detailed underlying mechanism is not clear at this point and requires further study, the experimental findings suggest that a gradual variation in the composition may yield a higher effective dielectric constant than when a homogeneously mixed state is produced under an identical average Hf:Al atomic ratio in the nanolaminated high-k film. As the measurement frequency decreases, the capacitance near the inversion region increases for both samples, as shown in Fig. 5. Considering the low intrinsic carrier concentration of InP (~10^7 cm^{-3} at room temperature [24]), the "false-inversion" behaviour observed indicates the presence and response of a large number of interface traps. The magnitude of the false-inversion decreased in the S1 sample when compared to that of the S2 sample, which matches with the increase in the Al_2O_3 concentration and also the decrease in the In incorporation near the interface region.

To provide a more quantitative comparison of the number of interface traps for the different nanolaminated samples that were engineered, frequency-dependent, parallel conductance (G_p) measurements were adopted by following the same procedure used in numerous reports [23,25]. Here, the maximum capacitance of the QSCV curves was used as the value for the oxide capacitance (C_{ox}) due to the difficulty in preparing inhomogeneous nanolaminate films of different thicknesses in order to extract the effective dielectric constant. Contour maps of the normalized parallel conductance ($G_p/A\omega q$, where A, ω, and q are capacitor area, angular measurement frequency, and elementary charge, respectively) are drawn as a function of the frequency and gate voltage measured for all samples in Fig. 6(a) and (b). A notable smear-out of the maximum $G_p/A\omega q$ peaks was observed for both samples throughout the depletion region, which is related to the surface potential fluctuation caused by a large distribution in the interface [25]. Regarding the interface state density (D_{it}), the S1 sample is expected to have a lower value than the S2 sample. Further insight into the D_{it} distribution in the InP band gap can be obtained by approximating the interface trap energy level (E_t) below the conduction band edge (E_C) of InP using the following formula [23]:

$$E_C - E_t = k_B T \ln\left(\frac{\upsilon_{th}\sigma N_C}{\omega}\right) \quad (1)$$

where k_B and T are the Boltzmann constant and the measurement temperature, respectively. Here, the density of states in the conduction band (N_C) is 5.7×10^{17} cm^{-3}, the average electron thermal velocity (υ_{th}) is 3.9×10^7 cm s^{-1}, and the capture cross section (σ) is 1×10^{-15} cm^2, as previously indicated with data for InP from the literature [25]. By reading the maximum $G_p/A\omega q$ value at each measured frequency and multiplying by 2.5, the D_{it} distribution within the upper region of the InP band gap was plotted for both of the nanolaminated dielectrics, as shown in Fig. 6(c). A lower number for D_{it} across the scanned region could be achieved for the S1 sample relative to that of the S2 sample, so enriching the interface region with more Al_2O_3 could minimize the incorporation of In and could also improve the interface quality, which is consistent with the results from other analyses. It is also important to characterize the sub-class of the near-interface defects associated with the hysteresis of the C–V curves. Fig. 6(d) shows the effective trap density per unit energy with respect to the gate voltage extracted from the difference in the capacitance of the forward and reverse C–V scans: $C_{rf}(V_g) = |C_r - C_f|$ [26]. The total trap densities (total integrated area under the curve) were quite similar for both samples at around 2.9×10^{12} cm^{-2}. However, two

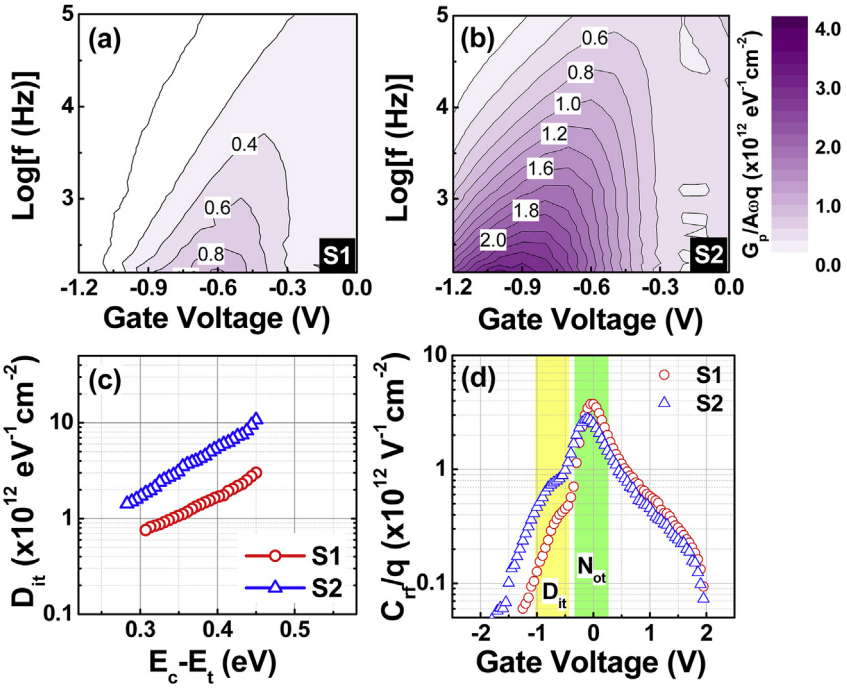

Fig. 6. Normalized parallel conductance ($G_p/A\omega q$) maps obtained from the (a) S1 and (b) S2 samples. (c) D_{it} distribution in the upper region of the InP bandgap for both samples. (d) Effective trap densities per unit energy as a function of the gate voltage for both samples, as calculated from the forward and reverse C–V curves measured at a frequency of 100 kHz.

distinct peaks can be observed in the depletion and in the accumulation regions, as shown in Fig. 6(d). The peak close to the depletion region is associated with the interface traps (D_{it}) and the peak in the accumulation region is related to the oxide traps (N_{ot}) [26]. The graded sample is confirmed to have a lower D_{it} than the homogeneous sample, which is consistent with the results obtained from the conductance measurements [see Fig. 6(c)]. However, this results in a slightly higher N_{ot}, which is probably due to the inhomogeneity in the film composition and may induce an increase in the number of bulk traps associated with the C–V hysteresis.

Fig. 7 shows the characteristics of the leakage current for two nanolaminated dielectrics in both polarities. Overall, the density of the leakage current for the uniformly nanolaminated sample (S2) is somewhat lower than that of the graded sample (S1), and this might be due to the difference in the spatial change in the band gap across the thickness corresponding to the compositional gradient. There is also a possibility of a slight difference in thickness (including the interfacial layer) between the samples. The degradation of the leakage current for the high-k dielectrics under electrical stress was further examined by measuring the repetitive leakage current curves under accumulation (positive gate bias) while the end voltage (V_{ramp}) increased in a stepwise manner [27], as shown in Fig. 8. When V_{ramp} is low, the leakage current curves shift continuously towards a higher voltage (marked as number 1 in the figure) due to charge (electron) trapping in the pre-existing traps within the dielectric. A further increase in V_{ramp} generated an irreversible stress-induced leakage current (SILC) (marked as number 2 in the figure), until a dielectric breakdown occurred (marked as number 3 in the figure). SILC is known to occur through the generation of neutral traps acting as electron transport sites [27], as demonstrated with an opposite shift in voltage in the leakage current curve. Interestingly, the initial electron trapping *via* pre-existing defects within the dielectric and the subsequent SILC generation were suppressed in the S2 sample when compared to the S1 sample, and this observation implies that the homogeneously-mixed HfO_2–Al_2O_3 dielectric can yield a higher resistive behaviour in the leakage current degradation during voltage stressing than for the graded nanolaminate dielectric. In our previous study, a similar phenomenon had also been observed in the stacked HfO_2/Al_2O_3 and in homogeneous HfO_2–Al_2O_3 dielectrics on $In_{0.53}Ga_{0.47}As$ substrates [14]. Although the exact underlying mechanism is not clear and requires further investigation,

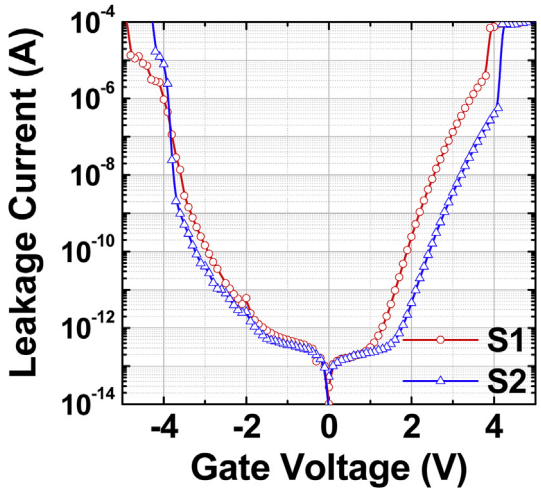

Fig. 7. Leakage current characteristics for the S1 and S2 samples in both polarities.

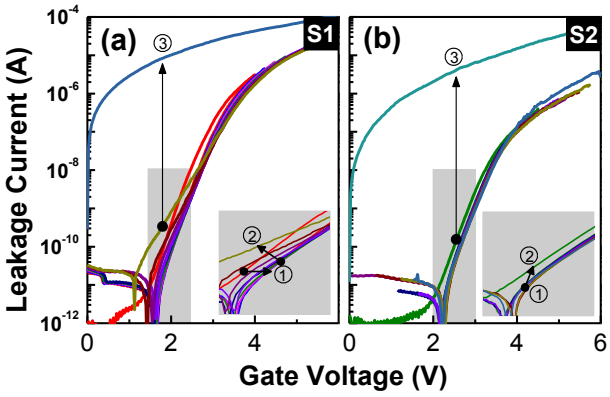

Fig. 8. Leakage current characteristics repeatedly measured with different ramp voltages, revealing the charge trapping characteristics under various applied voltages. The insets consist of enlarged graphs showing the direction of the shift in the leakage curve.

the observed difference may be related to the composition inhomogeneity of the film in a depth direction (e.g., more abundance of HfO_2 within the bulk region for the S1 sample than for the S2 sample).

4. Conclusion

In summary, we compared the electrical properties of nanolaminated HfO_2–Al_2O_3 films with different vertical compositional profiles on n-type InP substrates. The ALD processes were carefully scheduled in order to produce nanolaminated high-k films with graded composition (from HfO_2 to Al_2O_3 in the vertical direction on the substrate side) and uniform vertical composition profiles with similar physical thicknesses (5.3–5.5 nm) and CET (~1.8 nm). The graded sample with a higher Al concentration at the InP interface further minimized the amount of In incorporated within the interfacial region and reduced the D_{it} relative to those of the homogeneously-nanolaminated sample. In contrast, the leakage current and the trapping characteristics under a repetitive ramped voltage stress showed that the homogeneous HfO_2–Al_2O_3 film had a lower electron trap density and a better immunity to the SILC characteristics. Since the graded HfO_2–Al_2O_3 film has better interfacial characteristics with InP than the homogeneous film, it is believed that some compromise is inevitable in terms of its reliability, and further optimization including PDA under different condition is required for these materials to be used as a gate dielectric on III-V substrates.

Acknowledgements

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