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# Defect analysis and performance evaluation of p-type epitaxial GaAs layer on Ge substrate for GaAs/Ge based advanced device

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## ABSTRACT

The structural defects and formation of native oxides during thermal treatment on *p*-type epitaxial-GaAs/Ge have been investigated using spectroscopic measurements and electrical characterization. The performance of epi-GaAs based device depends on the interface quality between epi-GaAs and gate oxide and structural quality of the epi-GaAs layer. *P*-type epitaxial-GaAs was grown on Ge substrate using MOCVD technique at 675°C. Defective surface native oxides of arsenic and gallium oxides are observed for as-grown epi-GaAs layer. The arsenic oxide significantly reduced after thermal treatment as seen from XPS observations. The structural defects at surface enhanced after thermal treatment which is clearly probed by micro-Raman spectroscopy. Atomic layer deposited (ALD) $Al_2O_3$ significantly improved the interface properties after thermal treatment compared with bare epi-GaAs layer. Even though, the interface trap defect density slightly higher for *p*-type epi-GaAs MOS capacitor compared with bulk *p*-type GaAs devices, high frequency-dispersion in epi-GaAs based devices observed. This is mainly governs through the formation of *p-i-n* junction diode in the epi-GaAs layer on Ge substrates. Copyright © 2016 VBRI Press.

**Keywords:** GaAs; native oxides; Raman spectroscopy; rapid thermal annealing; GaAs/Ge integration.

## Introduction

It is of great interest to develop *p*-type epitaxial GaAs high mobility channel materials on the silicon (Si) platform to realize metal-oxide-semiconductor (MOS) devices with increased carrier mobility and device flexibility [**1-3**]. Epitaxial GaAs (epi-GaAs) on Ge substrate has received much attention to realize enhanced functionality of GaAs compounds coupled with the silicon-based process technology [**4-8**], where Ge layers are easily integrated with Si platform. However, device performance gains using *p*-type epi-GaAs/Ge layer have not been realized due to the deleterious effects from surface roughness of the epitaxial layer, poor native oxide quality, and structural defects in the epi-GaAs layer. Thus, it is critical to investigate the defects in the epi-GaAs layer to achieve high performance using GaAs/Ge based devices. In the present work, we have investigated the structural quality and interface properties of *p*-type epi-GaAs layer through spectroscopic analysis and electrical characterization to design the high quality p-type epitaxial-GaAs on silicon platform.

Epitaxial-GaAs directly on Ge suffers from poor surface quality with the presence of short range crystalline disorder. Ge out-diffusion and auto-*n*-type doping in the epi-GaAs is also critical for device applications [**9-12**]. Therefore, suppression of Ge out-diffusion and growth of high quality *p*-type epi-GaAs on a silicon platform is essential. On the other hand, surface oxide also plays a key role in the device performance. Unfortunately, native oxides of GaAs are responsible for the poor performance of the device. Thus, improvement of materials quality as well as reduction of surface native oxides is crucial to obtain the performance gains using epitaxial-GaAs. The surface oxides can be formed during thermal treatment of GaAs. In literature, the optical nondestructive probing studies of such GaAs/Ge subjected to thermal annealing are rather limited. Among various techniques, Raman scattering probes strain and crystal disorder in GaAs and addresses vibrational properties of such GaAs epitaxial layers. In addition, photoluminescence (PL) technique could probe optical properties in such GaAs/Ge system and related process-induced changes. In this work, we have studied the influence of thermal treatments on optoelectronic properties

 

of epi-GaAs layer by using x-ray photoelectron spectroscopy (XPS), PL, and micro-Raman analyses. Through electrical characterization, structural quality of the epi-GaAs has been evaluated.

## Experimental

The *p*-type epi-GaAs was deposited using a metal organic chemical vapor deposition (MOCVD) technique at 675 °C. A starting $Al_{0.3}Ga_{0.7}As$ buffer layer of 10 nm was used to suppress the Ge out-diffusion. An undoped GaAs intermediate layer with thickness of 300 nm was introduced between epi-GaAs and Ge substrate to reduce the intrinsic Ge auto-doping. The *p*-type epi-GaAs of ~ 200 nm was then overgrown on undoped GaAs. Schematic diagram of the epitaxial-GaAs layers was shown in **Fig. 1(a)**. Surface morphology of the epitaxial-GaAs was shown in **Fig. 1(b)**. After the MOCVD growth, the epitaxial-GaAs was subjected to rapid thermal annealing at 500 °C and 600 °C for 1 min in nitrogen ambient.

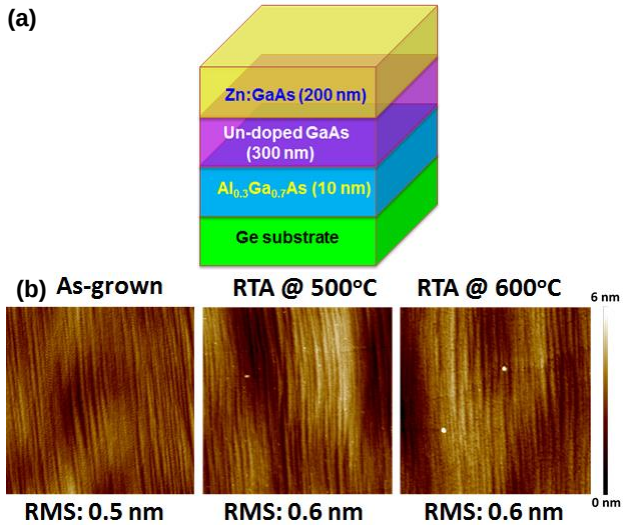


**Fig. 1.** (a) Schematic diagram of the epitaxial-GaAs layer used in this study. (b) AFM image of *p*-type epitaxial GaAs grown on Ge substrate with AlGaAs buffer layer. The surface roughness of epi-GaAs layer is ~0.5 nm. After thermal treatment, surface roughness slightly increases to 0.6 nm.

The surface morphology of epi-GaAs thin film was studied using Bruker Dimension Icon AFM system. The surface roughness of epitaxial-GaAs is ~0.5 nm and slightly increases to 0.6 nm after thermal treatment. Structural property of epi-GaAs was analyzed by micro-Raman spectroscopy using a JY LABRAM HR confocal Raman microscope equipped with a 488 and 325 -nm laser lines. In particular, to probe the nature of the top surface, 325 nm excited ultraviolet micro-Raman measurements are carried out. The formation of surface oxides and chemical composition of the epi-GaAs samples were examined by XPS using VG ESCALAB 220i-XL XPS system with monochromatic AlKa source (1486.6 eV). Electrical measurements were performed on GaAs metal-oxide-semiconductor (MOS) capacitor. Thin layer of $Al_2O_3$ was deposited on epi-GaAs layer by atomic layer deposition to fabricate epi-GaAs MOS structure. The Au metal, deposited by sputter, was used as the gate electrode (area: $1.9 \times 10^{-3}$ $cm^2$). Low resistance Ohmic contact was made by using Ti/Pt/Au on the back side of *p*-Ge wafers through sputter. Capacitance-voltage (C-V) and conductance voltage characteristics are measured using an Agilent B1500A semiconductor device analyzer. High-resolution transmission electron microscopy (HREM) was used to evaluate interface property between dielectric and epi-GaAs layer.

## Results and discussion

The chemical composition of epi-GaAs layer was studied by using XPS for as-grown and after thermal treatment of the epi-GaAs layer. To further investigate the chemical composition of the epi-GaAs surface and $Al_2O_3$/epi-GaAs interfacial structure was examined by XPS measurements. The Ga 3*d*, and As 3*d* core-level XPS spectra for both structures depicted in **Fig. 2** and **Fig. 3**, respectively. The peak at 19 eV is due to Ga-As bonds. It is clearly seen in the figure that the surface oxide is present. The presence of $GaO_x$ (Δ~0.8eV) and $Ga_2O_3$ (Δ~1.55eV) signal implies the existence of a Ga-O layer on epi-GaAs surface after thermal oxidation. There is a hump around ~20.5 eV which is related to the gallium oxide [**7, 13-14**]. It was observed that intensity of the gallium oxide increases with respect to that GaAs peak intensity with annealing temperature. As presented in the overall Ga3d spectra in **Fig. 2**, substantial amount of Ga oxides was generated accordingly through chemical transformation under higher temperature annealing condition. For the sample annealed at 600 °C, the intensity ratio of Ga-As: Ga-O bonding significantly lower compared with other samples.

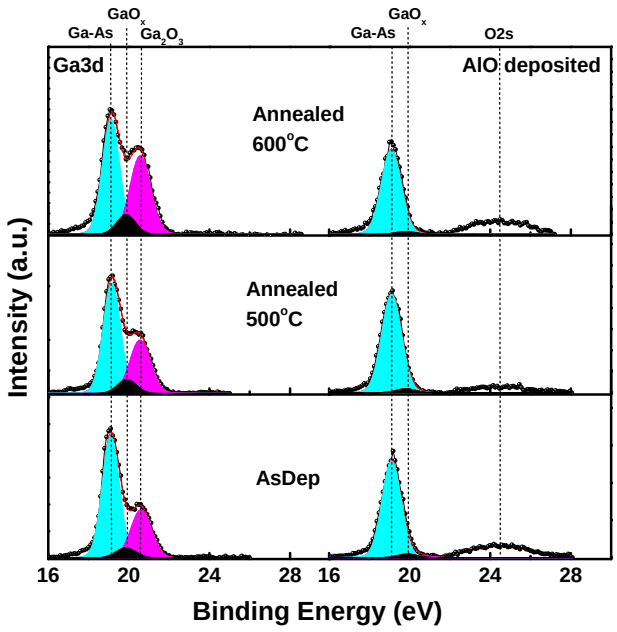


**Fig. 2.** Effect of thermal annealing at 500oC and 600oC for 1 min in nitrogen ambient on XPS core level spectra of Ga 3d before and after Al2O3 deposition.

This result suggests that the thickness of gallium oxides is increased. Thicker $Ga_2O_3$ layer on GaAs substrate shows

the considerably remaining on the GaAs surface because $Ga_2O$ is likely to convert to $Ga_2O_3$, due to the low thermal stability [**15**]. Therefore, it is concluded that the conventional thermal oxidation may not be an effective surface treatment for the GaAs surface states passivation. According to the Cheng *et al*. the Gibbs free energy ($\Delta G_f$) at room temperature is greater than zero as results the chemical reaction on GaAs surface does not occur [**16**]. But in higher temperature reaction kinetics changes and increases Ga-O formation. The growth of Ga–O oxide species existing near the ALD deposited $Al_2O_3$/epi-GaAs interface decreased after deposition as well as thermal post deposition annealing. **Fig. 2** shows that the substrate related oxides on the GaAs surface were effectively reduced by $Al_2O_3$ deposition due to the self-cleaning effect of TMA [**17, 18].** Gibb's free energy calculation attributes the passivation effect to the removal of Ga related oxide by the $Al_2O_3$ deposition. These results imply that it is not only $Al_2O_3$ deposition but even after subsequent thermal treatment up to 600 °C PDA leads to the stable interface on epi-GaAs. Above 24eV binding energy, a broad peak was observed after $Al_2O_3$ deposition which is originated from O-2*s* photoelectron signal observed overlapped with the Ga 3*d* core level spectra [**16**].

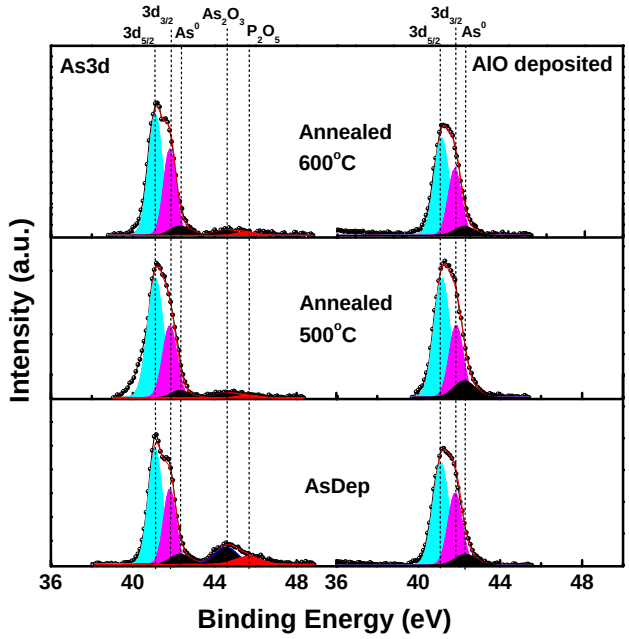


**Fig. 3.** Effect of thermal annealing at 500°C and 600°C for 1 min in nitrogen ambient on XPS core level spectra of As 3d before and after $Al_2O_3$ deposition.

**Fig. 3** shows the As 3*d* core level spectra of epi-GaAs surface as well as $Al_2O_3$/GaAs interface after thermal treatment at 500 °C and 600 °C along with as-deposited sample. The As 3*d* spectra consist of $As3d_{3/2}$, $As3d_{5/2}$ substrate peak along with arsenic oxides of $As_2O_3$, and $As_2O_5$ relative to their content in the as-deposited $Al_2O_3$ film. It was found that without annealing epi-GaAs surface was slightly oxidized because of transitory exposure to the ambient air. At a binding energy of 42.3 eV, elemental As ($As^0$) was occurred due to As bonded in bulk elemental As. The chemical shift of $As_2O_3$ and $As_2O_5$ relative to $As3d_{5/2}$ was 3.6 eV and 4.6 eV. Unlike to Ga3d spectra As-O slightly reduced after the rapid thermal annealing at high temperatures. The concurrent reduction of As-related oxide and oxidation of Ga is consistent with the conversion of arsenic oxide into gallium oxide at high temperatures. Thus, it is very essential to control the oxidation of GaAs surface during thermal treatment of the epi-GaAs layer. There are several approaches for surface passivation on the bulk-GaAs layer using dielectrics and interfacial passivation layer to reduce the interfacial native oxide formation [**19-30**]. The oxidation of gallium (Ga) during post deposition annealing of dielectric films are also observed in the case of both bulk-GaAs and epi-GaAs. However, the amount of oxidation is more for epi-GaAs when compared with that of bulk-GaAs substrates [**7**]. XPS spectra from **Fig. 3** indicate that the ALD $Al_2O_3$ layer is effective in blocking the diffusion of oxidizing species into the substrate. Nearly zero As-O peak was found after $Al_2O_3$ deposition which further confirms the Ga3d results discussed above. Though it cannot be ruled out the possibility that a tiny amount of As oxides diffused into the $Al_2O_3$ high-k film during deposition or annealing due to the limitation of sensitivity of the XPS measurement. Furthermore, after $Al_2O_3$ deposition negligible trace of elemental As was detected at the interface due to the exchange reaction between GaAs substrate and arsenic oxide [**19**].

The structural quality of the annealed p-type GaAs epilayers with and without $Al_2O_3$ high-k layer are studied by the behavior of optical phonon peaks in the Raman spectra. The atomic scale disorder caused by thermal annealing and related changes in the lattice parameters influences Raman spectral line shapes of GaAs. The strain usually leads to a shift in phonon frequency, change in the line width, and lattice disorder introduces disorder-activated modes or a breakdown of the Raman polarization selection rules. **Fig. 4(a, b)** show room temperature Raman spectra of epi-GaAs layer grown on a Ge substrate with the thin AlGaAs buffer layer.

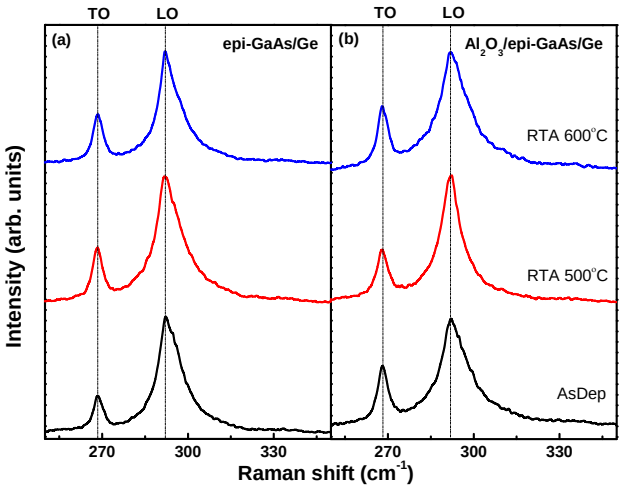


**Fig. 4.** Raman spectra of epitaxial-GaAs layer for as-grown and after thermal treatment (a) with and (b) without $Al_2O_3$ using 488 nm visible Raman excitation.

The Raman spectrum of as-grown GaAs layer and $Al_2O_3$ passivated GaAs shows both transverse optical (TO)

phonon at ~268 $cm^{-1}$ and a longitudinal optical (LO) phonon at ~293 $cm^{-1}$, similar to the reported results [**31, 32**]. In case of GaAs, the LO mode is Raman-active while the TO mode is sensitive to structural disorder, surface roughness, and impurities [**33, 34**]. The phonon peaks from the as-grown epilayer on Ge substrate shows a phonon hardening when compared to LO and TO phonon energies of bulk GaAs substrate. This is due to the lattice strain present in the epilayers, while thermal annealing is expected to create surface disorder due to presence of ultrathin oxide complexes as seen from XPS results. The LO phonon mode observed in the annealed layers is stronger and shifted to 291 $cm^{-1}$ due to relaxation of compressive strain component. However, the weaker TO phonon peak line which is forbidden in this Raman polarization configuration became intense and shifted to 266.5 $cm^{-1}$. The appearance of this symmetry-forbidden TO can arise from the deviation of backscattering configuration and breakdown of the long range order due to lattice distortion caused by thermal treatment. Since the intensity ratio between TO and LO, is small, the deviation from strict backscattering configuration should be small, which should not have significant influence on the electronic properties. After $Al_2O_3$ deposition, the Raman spectrum from as-grown layer shows a slight increase of TO-to-LO phonon intensity ratio. While after annealing no significant change is seen in the ratio (**Fig. 4(b)**). This implies a reduction of interface defects or absence of high density of dangling bonds with $Al_2O_3$ capping. The LO phonon peak of the as gown epi-GaAs is sharp while for sample annealed at 600 °C it shows a line broadening. This indicates an introduction of crystalline disorder at the surface as Raman technique probes the top p-GaAs due to penetration depth of the laser beam. The peak intensity for TO band increases with annealing temperatures and also the LO phonon line shows clear asymmetry toward the lower energy side. This could be related to the structural defects at the surface leading to line broadening at 600 °C while no significant LO phonon spectral line shape change at 500 °C.

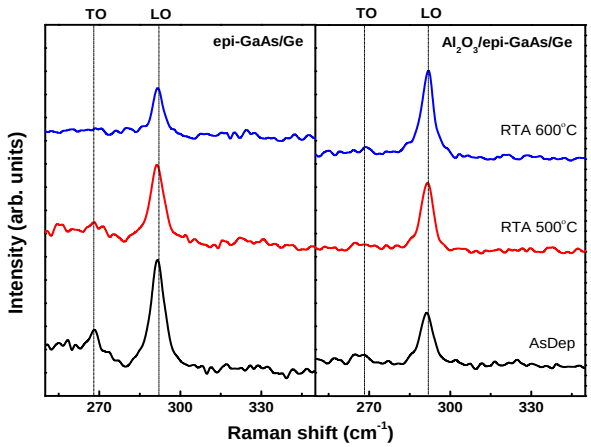


**Fig. 5.** Raman spectra of epitaxial-GaAs layer for as-grown and after thermal treatment (a) with and (b) without $Al_2O_3$ using 325 nm UV Raman excitation.

In order to probe the surface disorder-induced electronic properties, we have recorded 325 nm UV Raman spectra as shown in **Fig. 5**.

The UV laser probing depth is limited to the top p-GaAs surface layers <10 nm. The as-deposited p-type GaAs shows a gradual decrease of LO phonon intensity in the UV-Raman spectra from the surface due to increased disorder without dielectric capping. In contrast, with $Al_2O_3$ the LO phonon intensity increases with thermal treatment. This confirms the XPS observations where surface passivation helps to reduce out diffusion and improved the crystalline ordering of the top interface. Furthermore, the PL studies have been conducted in as-grown and annealed p-GaAs epi-layers on Ge substrate. The PL spectra of epi-GaAs layers measured at room temperature are presented in **Fig. 6**. Single PL peak representing GaAs near-band-edge emission suggests that there is no significant Ge diffusion into the epi-GaAs layer. The main peak at room temperature corresponds to an energy value of 1.415 eV while emissions from 1.2 to 1.3 eV related to Ge diffusion into GaAs is found out to be negligible [**4**].

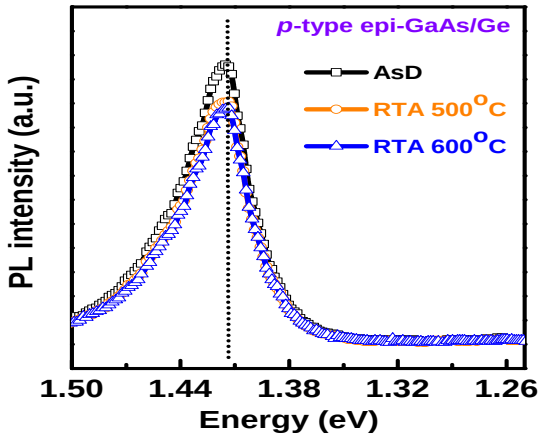


**Fig. 6.** PL spectra of epitaxial-GaAs layer for as-grown and after different annealing conditions.

The PL line width asymmetry change in annealed samples is also negligible when compared to as-grown sample. The PL peak shift is also very small (~2 meV) and rules out significant band gap changes associated with any lattice disorder. The small change in PL peak intensity in annealed samples is due to the change in the chemical bonding configurations at the surface as probed by the XPS technique. The surface disorder due to the As out diffusion changed crystal quality at the surfaces. As a result, PL intensity is slightly reduced after thermal treatment.

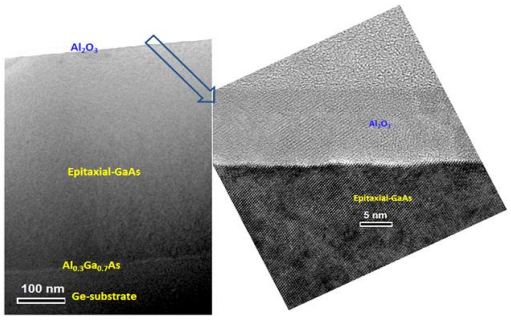


**Fig. 7.** Cross-sectional high-resolution TEM image of p-type epi-GaAs/$Al_{0.3}Ga_{0.7}As$/Ge with atomic layer deposited $Al_2O_3$ films of 12 nm. The gate $Al_2O_3$/p-type epi-GaAs/$Al_{0.3}Ga0.7As$/Ge structure annealed at 500°C for 1 min in rapid thermal system.

**Fig. 7** shows cross-section HRTEM image of epi-GaAs layer coated with ALD $Al_2O_3$. The total thickness of epi-GaAs layer is 490 nm. Thickness of $Al_{0.3}Ga_{0.7}As$ buffer layer is 9.8 nm. There was no indication of forming interfacial layer between *p*-type epi-GaAs and $Al_2O_3$, as shown in HRTEM image. This is due to the self-cleaning property of ALD $Al_2O_3$. The ALD process removes native oxide and excess As on GaAs surface, resulting almost no interfacial layer between $Al_2O_3$ and epi-GaAs layer.

Determination of $D_{it}$, the interface trap density and their trap level energy position is very important for high-k/III-V interface structures. During capacitance-voltage measurement DC bias is applied along with a small ac signal (~30 mV). Fermi level of the semiconductor and high-k interface strongly depends on the band bending or surface potential due to the applied voltage. The interface traps follow ac signal frequency and change their occupancy regarding to their response time (τ).

Conductance method deals with the loss related to trap level charge state variation. From conductance technique, $D_{it}$ can be measured along with the band bending and Fermi level movement directly from experimentally obtained C-V and G-V data. We have evaluated the interface property of the $Al_2O_3$/*p*-type epi-GaAs interface by using the capacitance-voltage (C-V) and conductance-voltage (G-V) characterization. For $Al_2O_3$/*p*-epi-GaAs structure, midgap interface trap density ($D_{it}$) can be obtained from conductance maps, which plot $G_p/A\omega q$ as a function of frequency and applied gate bias, where q is the elemental charge and $G_p$ is the parallel conductance. $G_p$ is obtained from the measured conductance ($G_m$) and the oxide capacitance density, $C_{ox}$. **Fig. 8** shows $G_p/A\omega q$ vs frequency plots for $Al_2O_3$/epi-GaAs MOSCAP. The parallel conductance $G_p/\omega$ is given by [**35**],

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (1)$$

The $D_{it}$ in depletion is proportional to the peak values of $G_p/\omega$. The trap energy level, i.e., the energy difference to the majority carrier band edge, ΔE, can be estimated from the relationship between the frequency '*f*' at which $G_p/\omega$ peaks has maximum loss and is given by,

$$\Delta E = kT \ln\left(\frac{\upsilon_{th}\sigma N}{\omega}\right) \quad (2)$$

where, *N* is the effective density of states of the majority carrier band, $v_{th}$ is the average thermal velocity of the majority carriers, and $\sigma$ is the capture cross section of the trap state, $k_B$ the Boltzmann constant, and *T* the absolute temperature. All values for $v_{th}$, *N*, and $\sigma$ were obtained from this analysis giving an average hole thermal velocity ($\upsilon_{th}$) of $1.8 \times 10^7$ cm $s^{-1}$, a capture cross section (σ) of $1 \times 10^{-15}$ $cm^2$, and a density of states in the valance band is (*N*) of $9.0 \times 10^{18}$ $cm^{-3}$ [**36**]. The position of the $G_p/A\omega q$ peak shifts along with the frequency as the gate bias changes. The peak shift indicates that the surface potential modulates efficiently relative to the gate bias when the Fermi level is located between valance band edge and midgap. The $G_p/A\omega q$ versus gate bias characteristics shows higher peak values at lower frequencies and almost no peak movement with gate bias at higher frequencies, which could be due to the onset of inversion, where the conductance is dominated by minority carriers or Fermi level pinning [**37**]. The final $D_{it}$ can be calculated from the expression,

$$D_{it} = 2.5\left(\frac{G_p}{A\omega q}\right)_{\max} \quad (3)$$

The minimum $D_{it}$ found in the structure was ~$8\times10^{12}$ $eV^{-1}cm^{-2}$, shown in **Fig. 8** inset, which is comparable to the $Al_2O_3$/bulk-GaA system [**13, 22, 30, 38**].

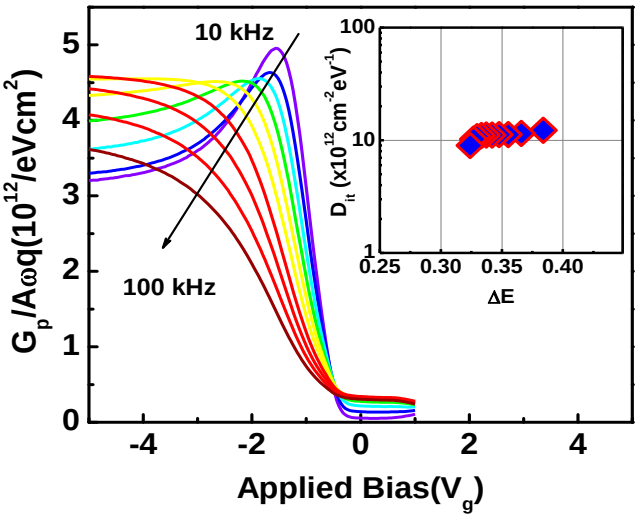


**Fig. 8.** Normalized parallel conductance map of $Al_2O_3$/epi-GaAs interface. The lines indicate the local $G_p/\omega$ maxima and trace of surface Fermi level. Inset shows the interface trap density.

It is worth to note that the $Al_2O_3$ was deposited without any surface passivation layer. Even though there is no significant interfacial layer formation between epi-GaAs and $Al_2O_3$, the $D_{it}$ is high which suggesting that the epi-GaAs surface quality further needs to be improved. The higher $D_{it}$ for epi-GaAs MOSC also possibly attributed to the high doping concentration in the epi-layer [**13**]. By reducing background doping due to the Ge diffusion (auto doping due to the Ge diffusion), it is possible to grow *p*-epi-GaAs with lower doping concentration. It is also worth to note that there is a significant impact on the gate oxide quality with germanium content in the channel layer [**39**]. Thus, for III-V/Ge based devices; it is desirable to suppress the background Ge content in the epi-GaAs layer [**40**].

**Fig. 9(a)** shows multi frequency C-V characteristics of epi-GaAs metal-insulator-semiconductor (epi-GaAs MIS) capacitor with 12 nm $Al_2O_3$ layer as a function of gate voltage. Very high dispersion appears in C-V characteristics at negative gate bias. The capacitance value decreases with increasing frequencies in negative gate bias conditions as seen in **Fig. 9(a)**. Even though interface trap density is comparable with the bulk GaAs based devices; high frequency dispersion is surprising. The possible

frequency dependent dispersion of C-V curve can be categorized by intrinsic and extrinsic reason. Extrinsic causes can be listed as lack of back contact and substrate series resistance. In our experiments, we have used Au back contact so this reason can be ruled out. Another extrinsic reason is formation of lossy interfacial layer, but from the HRTEM image we confirmed that our $Al_2O_3$/epi-GaAs has no interfacial layer (**Fig. 8**). Large frequency dispersion can also be for high surface roughness of the epitaxial layer. However, In **Fig. 1(b)** we already have reported that RMS value of the epi-GaAs was ~0.6 nm which is very similar to the bulk-GaAs substrate. Thus it is surprising to observe high frequency dispersion in accumulation region. Thus, for *p*-type epi-GaAs based MOS devices, it is necessary to understand the possible reason for the high frequency dispersion to grow the high quality epi-GaAs with minimum dispersion.

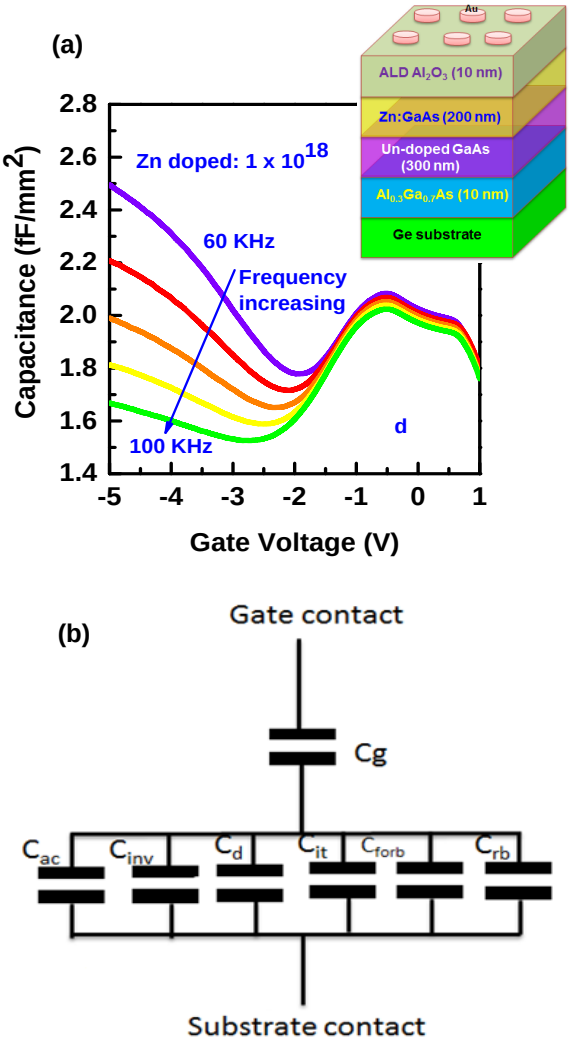


**Fig. 9**. (a) Multi-frequency Capacitance –Voltage 12 nm-thick unannealed ALD-grown Al2O3 films on p-type epi-GaAs. The bias voltage is swept from inversion to accumulation. (b) Capacitance equivalent circuit for the heterojunction epi-GaAs MOS capacitor.

The epi-GaAs MIS capacitor structure consists of *n*-type AlGaAs followed by undoped and *p*-dope GaAs which eventually form p-i-n heterostructure on Ge substrate, as shown in insert of **Fig. 9(a)**. The gate metal contact (Au) and substrate are separated by the insulator layer, the channel, the depletion region and junction. Hence, the total capacitance of the MIS structure can be represented as a series connection of the insulator capacitance, $C_g$, and the capacitance of the active semiconductor layer, $C_s$. The semiconductor capacitance depends on gate bias and applied frequency. The components of semiconductor capacitance can be represented as the sum of capacitances such as (i) accumulation capacitance, $C_{ac}$, (ii) inversion capacitance, $C_{inv}$, (iii) depletion layer capacitance, $C_d$, (iv) interface trap capacitance, $C_{it}$, (v) p-n junction capacitance at forward bias, $C_{forb}$ and (vi) reverse bias, $C_{rb}$, as shown in **Fig. 9(b).** There are two phenomena occurs when negative bias (-5V) apply to the gate. Firstly a strong accumulation of free majority carriers (holes) at $Al_2O_3$/*p*-type epi-GaAs interface occurs and secondly the maximum depletion of *p-i-n* junction formed as the junction is in reverse bias state. At this stage the junction capacitance approaching its smallest value due to the maximum depletion layer width and hence the total capacitance $C_{total} = \frac{C_g + C_{rb}}{C_g \times C_{rb}}$ is lower than gate oxide capacitance. From experimental data, it is obvious that the depletion width of *p-i-n* structure dominantly responsive over the MIS accumulation capacitance, which causes C-V characteristics similar to MIS capacitor being biased at depletion state even though MIS structure is in accumulation state at 100 KHz. With the positive gate bias, the free majority carriers (holes) will deplete from $Al_2O_3$/*p*-type epi-GaAs interface and create inversion/depletion layer below $Al_2O_3$ layer on *p*-type epi-GaAs surface, while the *p-i-n* junction will be at forward bias state. In forward bias, the junction depletion width reduces significantly which is responsible for larger junction capacitance $C_{forb}$. The experimental C-V curve shows that capacitance value is higher at positive gate bias than negative which indicates that total capacitance $C_{total} = \frac{C_g + C_{forb}}{C_g \times C_{forb}}$ is again dominated by the junction depletion width than depletion capacitance by MIS structure at 100 KHz. A plateau is observed at 0 to -0.5V gate bias. Noteworthy to mention that the flat band voltage is around -2.5 V and relative positive gate bias causes holes to drift from $Al_2O_3$/*p*-type epi-GaAs interface towards substrate and will be confining at the valance band offset of the heterostructure interface. Accumulation of positive free carries occurs during negative gate bias at $Al_2O_3$/GaAs interface while the *p-i-n* junction is in reverse bias and depletion layer start to increase with negative gate bias. Due to the depletion region expansion more carriers (electron hole pairs) are being thermally generated. The variation of accumulated positive free carrier charge at the $Al_2O_3$/*p*-type epi-GaAs interface proceeds at a rate limited by the time constants associated with the generation/recombination processes at the depletion region in *p-i-n* junction. The capacitance value with frequency indicates the response rate of carriers on ac signal and at this point, thus C-V frequency dispersion is observed.

## Conclusion

In summary, we have studied the impact of thermal annealing on structural and electronic properties of *p*-type

epi-GaAs layers grown on Ge substrate. The crystalline and surface oxidation properties have been studied using spectroscopic measurements. Formation of arsenic oxide and gallium oxides are observed for as-grown epi-GaAs layer. Arsenic oxide significantly reduced after thermal treatment as seen from XPS observations. There is no significant impact on the photoluminescence properties of epi-GaAs layer. The structural defects at surface enhanced after thermal treatment which is clearly probed by micro-Raman spectroscopy. With passivation by $Al_2O_3$, the interface properties improved after thermal treatment. The defect density slightly higher for epi-GaAs MOS capacitor compared with bulk-GaAs devices. Frequency-dispersion in accumulation regions are mainly governs through the p-in junction diode formation in epi-GaAs layer. Thus, for the epi-GaAs based logic and memory devices, it is necessary to reduce the impact of p-i-n diode on the MIS performance.

### Author's contributions

Conceived the plan: G.K.D.; Performed the experiments: G.K.D., V.S., S.C., Y.R., T.B., C.M.; Data analysis: G.K.D., V.S., C.M., T.B., S.T., T.L., D.Z.C, L.K.B.; Wrote the paper: G.K.D, C.M., S.T., L.K.B. Authors have no competing financial interests.

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